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JAN 78 D C CLAXTON, T D LEISHER, T G MILLS N00014-76-C-0570

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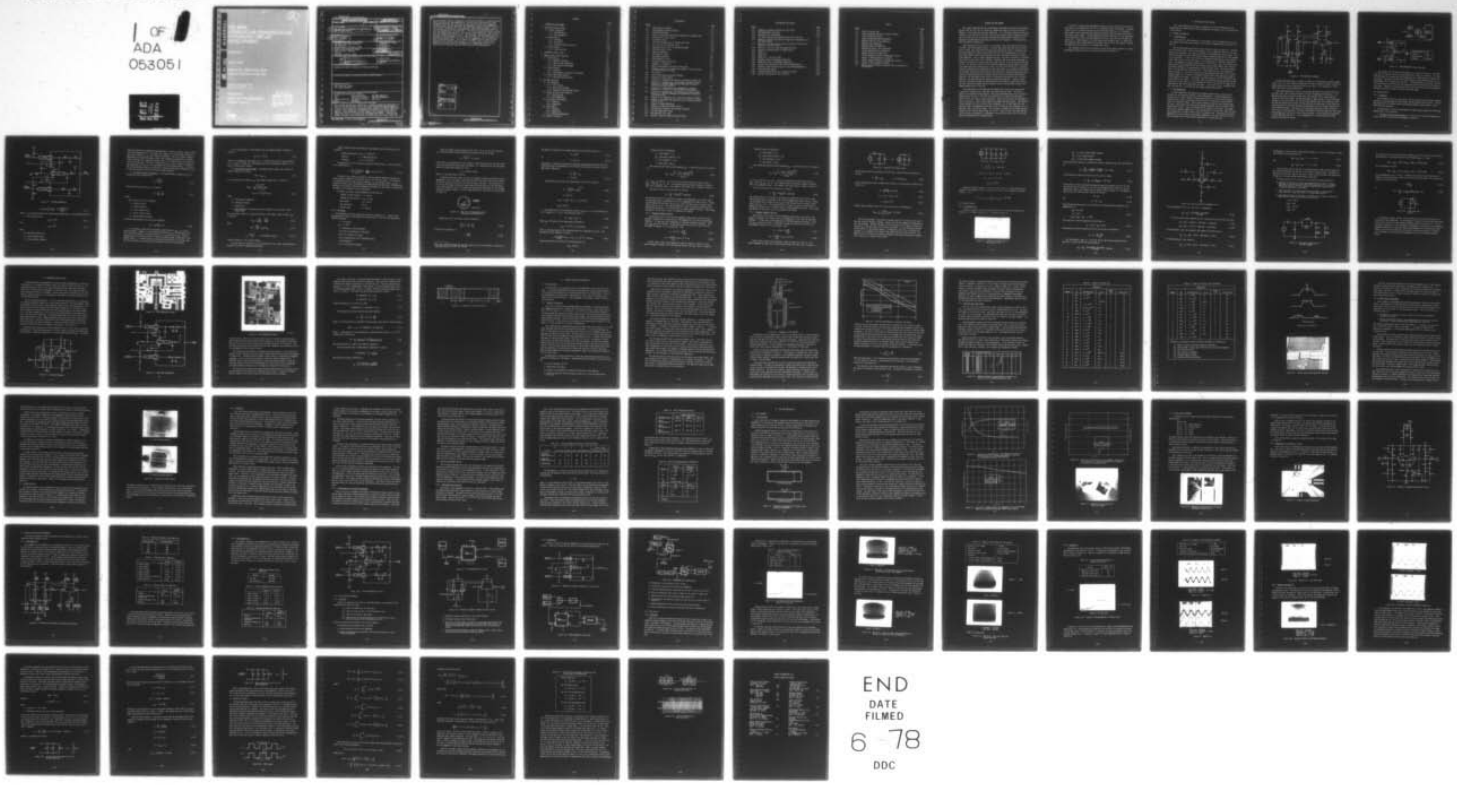

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This program had two basic objectives: to develop processing techniques suitable for the fabrication of small scale gallium arsenide (GaAs) integrated circuits, and to fabricate and evaluate GaAs biphase shift-keyed (BPSK) integrated circuit modulators and demodulators operating at 5 GHz carrier frequencies. GaAs integrated circuits require, as a minimum, field effect transistors (FET's), resistors, and interconnection metals. Previous TRW studies had shown that the addition of planar, gate controlled transferred

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electron devices (TED's), capacitors, and multilevel metals for undercrossings would facilitate the implementation of circuits which could perform useful microwave functions with a low device count and at fairly high frequencies. The design goals for the modulator and demodulator circuits were operation at 5 GHz carrier frequency and 1 Gbps data rate with minimum dc power. The circuit designs are distinctly nonconventional, having been developed specifically for implementation with the TED's. The TED's are used basically as phase logic AND gates, while the FET's are used as linear amplifiers. Both circuits generally exceeded the design goals: the modulator circuit operates from 4.5 to 8 GHz carrier frequency, 0 to 1.4 Gbps data rate, and 440 mW dc power; the demodulator operates from 4 to 10 GHz carrier frequency, 0 to 1.6 Gbps data rate, and 235 mW dc power. The IC chips are roughly 75 mils square and are mounted in test fixtures whose volume is 0.75 in^3. These circuits both represent new state of the art performance for integrated circuits of any type as well as for high data rate BPSK modulators and demodulators.

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ILLUSTRATIONS (Continued)

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1. INTRODUCTION AND SUMMARY

This report summarizes the work performed by TRW Defense and Space Systems between February 1976 and July 1977 on Contract No. N00014-76-C-0570 for the Office of Naval Research. This program had two basic objectives: (1) to develop processing techniques suitable for the fabrication of small scale gallium arsenide (GaAs) integrated circuits, and (2) to fabricate and evaluate GaAs biphase shift-keyed (BPSK) integrated circuit modulators and demodulators operating at 5 GHz carrier frequencies. These objectives were successfully accomplished.

GaAs integrated circuits require, as a minimum, field effect transistors (FET's), resistors, and interconnecting metals. Previous TRW studies had shown that the addition of planar, gate controlled transferred electron devices (TED's), capacitors, and multilevel metals for undercrossings would facilitate the implementation of circuits which could perform useful microwave functions with a low device count and at fairly high frequencies. Each of these components existed in one form or another as a discrete device prior to the start of this program. Therefore, the chief process development task was to establish a process which would allow them all to be fabricated on the same IC chip. For the TED's and FET's, this involved establishing designs which allow both to be fabricated on the same epitaxial layer. For the thin film resistors, a material (CrGe) was developed which adheres well to the GaAs, which can be etched without attacking the GaAs, and which can withstand the heat required in subsequent processing steps. Parallel plate metal-oxide-metal (rather than the lossier metal-oxide-semiconductor capacitors were developed using aluminum as the metal and anodized as the insulating material. The same technique was used to provide undercrossings. Finally, a chip-substrate interconnect scheme was developed which uses coplanar transmission lines on the chip interfacing between matching coplanar lines on the substrates and the first lumped element device on the chip.

The design goals for the modulator and demodulator circuits were operation at 5 GHz carrier frequency and 1 Gbps data rate with minimum dc power. The circuit designs are distinctly nonconventional, having been developed specifically for implementation with the TED's. The TED's are used basically as phase logic AND gates, while the FET's are used as linear amplifiers. These circuit designs are described in detail in Section 2. Both circuits generally exceeded the design goals: the modulator circuit operates from 4.5 to 8 GHz carrier frequency, 0 to 1.4 Gbps data rate, and 440 mW dc power; the demodulator operates from 4 to 10 GHz carrier frequency, 0 to 1.6 Gbps data rate, and 235 mW dc power. The IC chips are roughly 75 mils square and are mounted in test fixtures whose volume is 0.75 in^3. These circuits both represent new state of the art performance for integrated circuits of any type as well as for high data rate BPSK modulators and demodulators.

In spite of the excellent performance of these circuits, neither could be considered ready in its present state for use in a deliverable piece of hardware. The demodulator circuit is currently too dc-bias and input-level sensitive. In retrospect, these sensitivities could have been reduced by improving the TED design, specifically with shorter gate lengths. The BPSK modulator exhibits rather poor carrier suppression (10 to 20 dB) due to poor isolation between the carrier input port and the modulated output port. A minor change in the chip layout could be made to move the output coupling capacitors much further away from the input lines to solve this problem. Shorter TED gates would also be useful in the modulator circuit.

The following sections give the details of the circuit design (Section 2), process development (Sections 3 and 4), and the RF test results (Section 5).

2. DEVICE AND CIRCUIT DESIGN

This section describes the theory of operation of the TED BPSK modulator and demodulator and presents details of the assumptions and methods used in the device and circuit design.

2.1 THEORY OF OPERATION

2.1.1 BPSK Modulator

The function of a BPSK modulator is to multiply a carrier frequency by a digital data stream and provide phase changes in the carrier corresponding to the digital "1"s and "0"s.

The TED BPSK modulator designed on this program is shown in Figure 2-1. Ignoring the FET portion of the circuit for the moment, it can be seen that the TED's are used basically as AND gates. One input to each TED is the unmodulated carrier signal. The TED's are designed to have a transit-time frequency approximately equal to the intended carrier frequency. If one of the TED's has a negative voltage applied to one gate and an RF signal applied to the other gate, it will operate as an injection-locked oscillator. The negative resistance characteristic of the TED will cause the voltage at its anode end to be approximately 180° out-of-phase with the input signal, while the voltage at the cathode end is approximately in-phase with the input. The phase differential at the two ends will be exactly 180°. If two identical TED's are arranged as shown in Figure 2-1, one with an output from the cathode and the other with an output from the anode, and if a means is provided to control which TED supplies the output, a BPSK modulator is formed. The control is accomplished via the FET differential amplifier shown in the figure. If the data input is a positive voltage, the drain on the right FET is driven negative, activating the left TED and causing the RF output to be approximately 180° out-of-phase with the input. If the data input is a negative voltage, the other TED is activated and the output changes phase by 180°.

2.1.2 BPSK Demodulator

The GaAs demodulator developed on this program employs both a unique circuit design and a new conceptual approach to BPSK demodulation. Coherent demodulation involves one of several methods of reconstructing the carrier from the received suppressed carrier signal, and phase-locking the carrier to (making it phase coherent with) the transmitter signal. Once a phase coherent carrier has been reconstructed, the data is recovered by multiplying the incoming suppressed carrier spectrum by the reconstructed carrier. One of the multiplication products is the data. The cumbersome part of coherent demodulation is the reconstruction of the carrier, which is normally accomplished in either a Costas loop or a squaring loop. Differentially coherent demodulators are much simpler than coherent demodulators, but have inferior bit error rate performance and are restricted to operation at a single data rate.

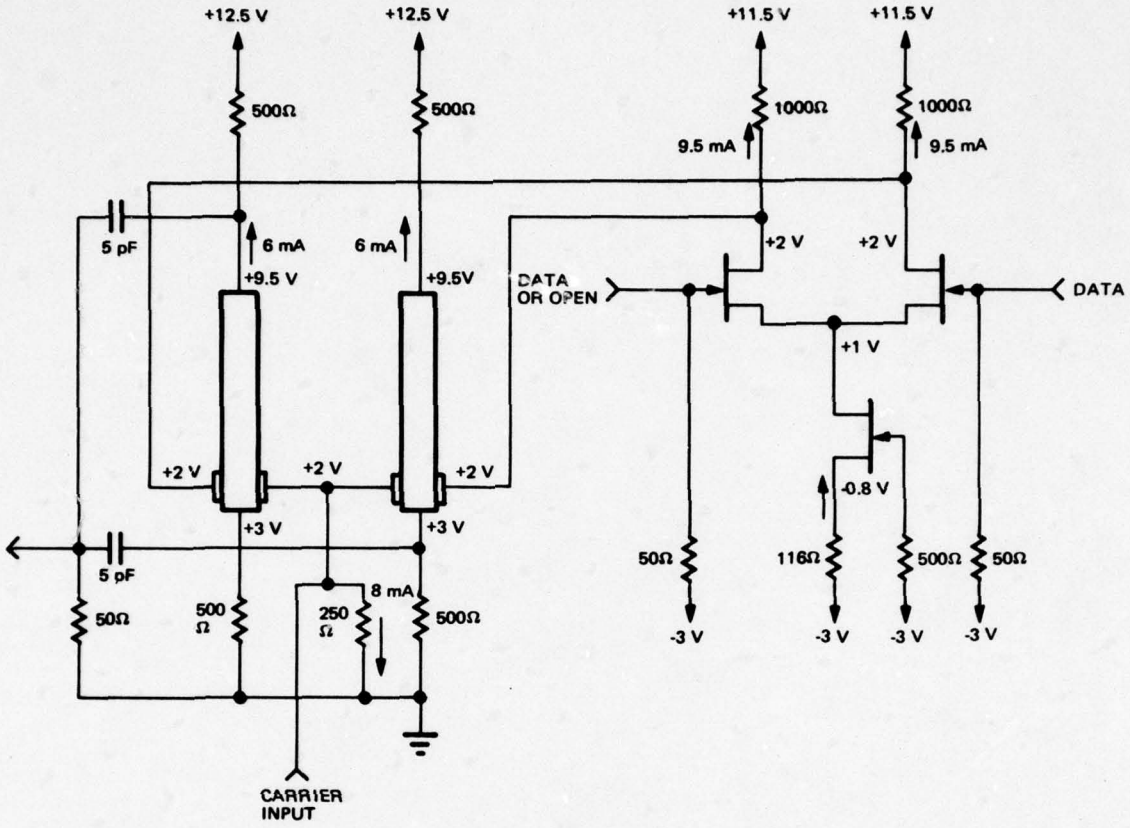

Figure 2-1. BPSK Modulator Schematic

The GaAs BPSK demodulator is nearly as simple as a differentially coherent demodulator, but is in fact a coherent demodulator in which an injection-locked, rather than phase-locked, oscillator reconstructs the carrier signal. This technique is called phase logic BPSK (PL-BPSK) demodulation.

The PL-BPSK demodulator (Figure 2-2) uses two AND gates which operate with phase scripted logic, and an injection-locked oscillator to demodulate BPSK signals. The AND gates provide an output when both inputs are in-phase, and no output when the inputs are 180° out-of-phase. The AND gate outputs, when present, are amplified reproductions of the input signal, and thus are phase coherent with the transmitted signal. The AND gate whose input has been satisfied provides an input signal to the injection-locked oscillator so that the injection-locked output will also be phase coherent with the transmitted signal. The outputs of the injection-locked oscillator provide the other inputs to the AND gates. The phase relationships around the upper and lower loops are arranged such that the oscillator injecting signal is at the same phase regardless of which AND gate provides it. The data demodulation is accomplished by envelope detecting the AND gate outputs.

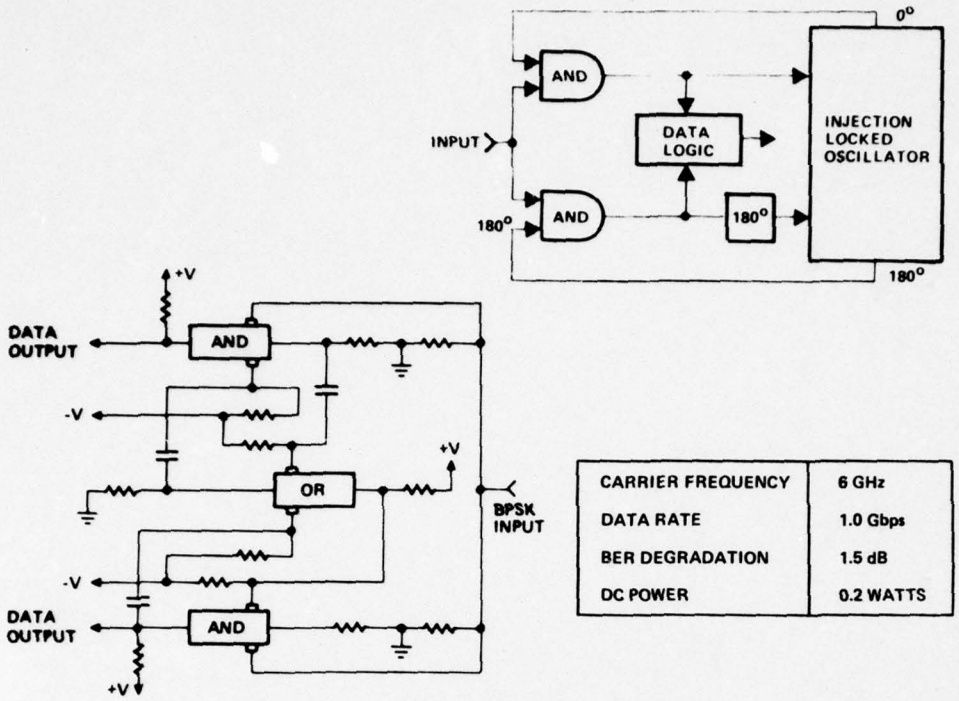

Figure 2-2. BPSK Demodulator Design and Goals

The schematic for the TED PL BPSK demodulator is shown in Figure 2-3. The AND gate TED's on the left provide RF outputs when their inputs are in-phase. The output from the upper TED is taken from the cathode end and is approximately in-phase with the inputs. The output from the lower TED AND gate is taken from the anode end and is approximately 180° in-phase with its inputs. The AND gate whose inputs are satisfied will injection-lock the third TED (the injection-locked oscillator) which functions as an OR gate. Outputs are taken from both ends of the oscillator and are phased appropriately to provide the other two inputs to the AND gates.

2.2 DEVICE DESIGN

2.2.1 TED Design

The dual-gate planar TED is basically a planar Gunn device with two ohmic contact terminals, called the anode and the cathode, and two Schottky barrier gates. The dual-gate planar TED is fabricated from an N-type GaAs epitaxial layer grown on a semi-insultaing GaAs substrate.

In the design of a TED, the requirements of primary concern generally include the determination of the following:

1) The domain transit time frequency. On the basis of previous measurements on 3 and 5 GHz TED's, the transit time frequency is given by

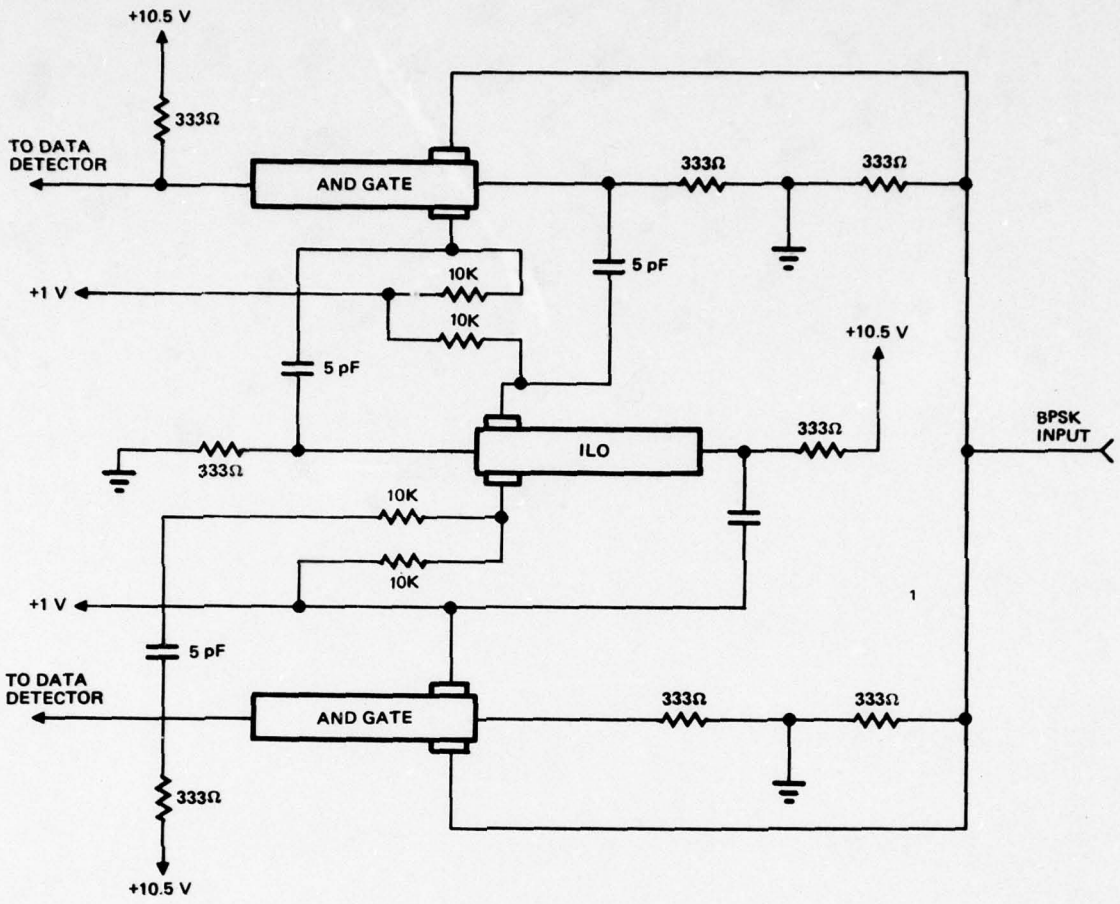

Figure 2-3. TED BPSK Demodulator

$$f = \frac{1.26 \times 10^7 \text{ cm/sec}}{\ell} \cdot \frac{\mu_m \text{ (measured)}}{8000} \qquad (2.1)$$

where ℓ is the distance between the cathode and the anode and μ_m is the measured mobility.

2) The conditions that

$$n_o \ell_t \geq 10^{13} \qquad (2.2)$$

and

$$n_o d \geq 10^{12} \qquad (2.3)$$

where

n_o = electron concentration

ℓ_t = active channel length

d = active channel thickness

These two conditions are determined experimentally in order to achieve a large current drop after threshold occurs in a planar TED. However, for minimum power dissipation and trigger voltage, n_o, ℓ_t, and d should be minimized. The active channel length is determined by the specified domain transit time frequency and should have a minimum length sufficient for a domain to build up after it is launched either at the cathode or at the trigger gate. The lower limitation for $n_o d$ is that n_o should be chosen so that equations (2.2) and (2.3) are satisfied for a given channel length. In addition, the channel thickness should be sufficient to provide stable domain propagation because of the two-dimensional effects of the dipole domain formation.

3) The threshold power consumption. The threshold power consumption P_o for a two-terminal TED is determined by

$$P_o = \frac{E_{th}^2 \ell_t^2}{R_o} \tag{2.4}$$

and the low field resistance, R_o, is equal to

$$R_o = \frac{1}{q\mu n_o} \frac{\ell_t}{wd} \tag{2.5}$$

where

E_{th} = electric field at threshold

q = electron charge

μ = electron mobility

w = active channel width

ℓ_t = active channel length

d = active channel thickness

By substituting equation (2.5) into (2.4) we obtain

$$P_o = q\mu n_o E_{th}^2 \ell_t wd \tag{2.6}$$

It is, therefore, seen that for minimum P_o, small values of n_o, ℓ_t, w, and d should be chosen, However, for satisfying the conditions $n_o \ell_t \geq 10^{13}$ and $n_o d \geq 10^{12}$ for a specified frequency, the lower limits for n_o, ℓ_t, and d are fixed. The only parameter that we can reduce which will lower the threshold power consumption is the channel width, w. It should be borne in mind that the reduction of w increases the low field resistance, R_o, which may not be desirable for circuit applications.

For a three-terminal or four-terminal TED, the threshold power consumption is given by

$$P_{oG} \simeq (1 - X)^2 P_o \tag{2.7}$$

where X is the depletion layer depth at Z = 0 divided by the active layer thickness, or $X = (\phi_d/\phi_p)^{1/2}$, where ϕ_d is the voltage drop across the depletion layer at Z = 0, and ϕ_p is the pinchoff voltage.

4) The minimum trigger voltage. The minimum input voltage, ΔVm, required for stable triggering is given by

$$\Delta Vm = \Delta_{min} \ell_t \tag{2.8}$$

for a two-terminal TED, where Δ_{min}, the minimum trigger field, is given by

$$\Delta E_{min} = \frac{q^{3/4} n_o^{3/4}}{K^{3/2} \varepsilon^{5/4} (kT_e)^{1/4}}$$

$$\simeq 1.5 \times 10^{-10} n_o^{3/4} \text{ (V/cm)} \tag{2.9}$$

where

T_e = the electron temperature

k = Boltzmann constant

ε = permittivity

K = the dimensional fluctuation due to the thermal noise normalized to the Debye length

For a TED with a single or a dual-gate structure, the minimum trigger voltage, ΔV_{mG}, is equal to

$$\Delta V_{mG} = \frac{\Delta V_m}{\ell_t \text{ hgs}} \quad \frac{\Delta E_{min}}{\text{hgs}} \tag{2.10}$$

where

$$\text{hgs} = \frac{\eta m E_{th}}{2\phi} \quad \frac{1}{X(1 - X)} \tag{2.11}$$

$$\phi_p = \frac{q n_o d^2}{2\varepsilon} \quad , \quad \text{the pinchoff voltage} \tag{2.12}$$

η and m are equal to 1 for a proper design.

As can be seen from equation (2.9), the reduction of the trigger voltage requires the use of low carrier concentration materials.

Based on meeting these considerations, the material for the TED design can be specified:

Doping concentration = $N_o = 7 \times 10^{15}$ cm^{-3}

Mobility = $\mu = 6200$ cm^2/volt-sec

Thickness = $d = 1.5 \times 10^{-4}$ cm

From equation (2.1) and the specifications of the epi-layer, ℓ can be calculated for a 5 GHz device as

$$\ell = \frac{1.26 \times 10^7 \text{ cm/sec}}{5 \times 10^9 \text{ Hz}} \cdot \frac{6200}{8000} = 19.53 \times 10^{-4} \text{ cm} \qquad (2.13)$$

The width of the channel was chosen to provide the best compromise between the desired power consumption of the device and its low field resistance. The separation of the Schottky barrier gates from the cathode, ℓ_{cg}, and the gate length, ℓ_g, was minimized to reduce power dissipation and trigger voltage, respectively. These minimum distances are limited by the photolithographic techniques but the separation between the two gates is not important for this application.

In summary, the device design parameters for the TEDs are:

Cathode to anode distance = ℓ = 19.5 μm

Cathode to gate distance = ℓ_{cg} = 3.0 μm

Gate length = ℓ_g = 3.0 μm

Gate separation = 4.0 μm

Channel width = w = 26.0 μm

2.2.2 FET Design

The parameters of the epi layer were specified in Section 2.3.1. Based on this and previous FET designs, the quiescent bias conditions for the FET's were determined from the following:

d = 1.5 microns

$N_o = 7 \times 10^{15}$

1 V reverse bias TED gate/channel

0.6 V built-in potential for TED gates

0.4 V p-p voltage at FET input

0.5 p-p voltage swing at FET output/TED input

1.25 voltage gain

5 x 11 μm TED gate structures

Using the graphic design approach of R.B. Fair,* 5 x 11 μm, we first calculate V_o, the total pinchoff voltage including the barrier voltage of the gate

$$V_o = \frac{q N_o d^2}{2\varepsilon} = 12.9 \text{ volts}$$

From a minor of extrapolation of Fair's Figure 6, plus corrections for FET gate length (3 μm) and the extrinsic gate-source resistance, it is determined that the transconductance for a gate-source spacing of 3 μm is

$$g_m = 0.024Z \text{ millimhos}$$

where Z is the gate width in microns.

To determine the gate width, the gain and frequency response requirements must be determined. It will be shown in the next section that the equivalent RC time constant of the FET output circuit must be less than or equal to 64 psec. The capacitive portion of the FET output includes the capacitance of the TED gate plus the capacitance of the interconnecting line. To estimate the edge effect capacitance for the Schottky structure, Poisson's equation is first solved for the full cylindrical structure shown in Figure 2-4.

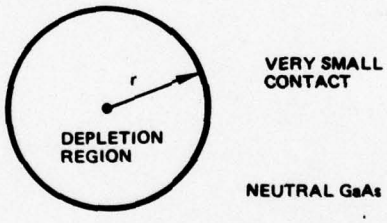

Figure 2-4. Model for Estimating Edge Effect Capacitance of Schottky Gate

Neglecting Z and θ variations, Poisson's equation is

$$\frac{\partial^2 \phi}{\partial r^2} + \frac{1}{r} \frac{\partial \phi}{\partial r} = \frac{qN}{\varepsilon \varepsilon_o} \tag{2.15}$$

Solution to the equation is

$$\phi = \frac{qNr^2}{4\varepsilon\varepsilon_o} \tag{2.16}$$

*R.B. Fair, "Graphical Design and Iterative Analysis of the DC Parameters of GaAs FET's," IEEE Trans. E.D., June 1974, pp. 357-362.

The amount of charge per unit length contained in the depletion region is

$$Q = qN\pi r^2 \tag{2.17}$$

or

$$Q = 4\pi\epsilon\epsilon_o \phi \tag{2.18}$$

Each edge of a Schottky structure has a depletion region outside the parallel plate region which may be represented as 1/4 of the full cylindrical structure, giving an edge effect capacitance

$$C = \frac{1}{4} \frac{\partial Q}{\partial \phi} = \pi\epsilon\epsilon_o$$

$$\doteq 3 \text{ pF/cm} \tag{2.19}$$

The depletion region under the Schottky gate of the TED is given by

$$W = \frac{2\epsilon\epsilon_o}{qN} \left[(V + V_B)\right]^{1/2} \tag{2.20}$$

$$W \simeq 0.53 \ \mu m$$

$$C_{TED} = \epsilon\epsilon_o \frac{Z\ell}{W} + 2\pi Z\epsilon\epsilon_o = \epsilon\epsilon_o Z \left(2\pi + \frac{\ell}{W}\right) \tag{2.21}$$

$$C_{TED} \simeq 0.017 \text{ pF}$$

The voltage gain of the differential stage is $g_m R_L/2$, so if the minimum gain of 1.25 is chosen, $R_L = 2.5\ g_m$. The capacitance load is

$$C_L = C_{TED} + C_{gd} + C\ell \tag{2.22}$$

where C_{gd} = FET gate to drain capacitance, estimated at

$$C_{gd} = 3 \times 10^{-4}\ Z \text{ (Z in microns)} \tag{2.23}$$

and $C\ell$ is the capacitance of the interconnecting line, estimated at 0.01 pF. The equivalent RC time constant is given by

$$\tau = \frac{2.5 \times 10^3}{0.024Z} (0.017 + 0.01 + 3 \times 10^{-4}\ Z) \leq 64 \text{ psec} \tag{2.24}$$

Taking the equality and solving for the minimum value of Z

$$Z_{min} = 85.8 \ \mu m$$

Summarizing the FET dimensions,

L_g = gate length = 3 μm

L_{gs} = gate-source spacing = 3 μm

d = epi thickness = 1.5 μm

Z = gate width = 100 μm

Now estimating the drain current assuming V_{gs} = -4 volt and using Fair's equation (11)

$$I_{DS} = I_{DSS} \frac{\left[1 - \left((V_G + V_B)/V_o\right)^{1/2}\right]}{1 - (V_B/V_o)^{1/2}} \tag{2.25}$$

V_G = 4, V_B = 0.6, and V_o = 12.9. From Fair's equation (25) and Figures 4 and 5, I_{DSS} = 18.62 and I_{DS} = 9.5 mA. This completes the calculations necessary to define the circuit component values. The schematic with these values is shown in Figure 2-1.

The value of the FET drain resistors is given by

$$R_L = \frac{2.5}{g_m} = \frac{2.5 \times 10^3}{2.4} \simeq 1000 \text{ ohms} \tag{2.26}$$

The current source FET is basically the same as the differential pair FET's except that the gate width is increased to 150 μm to accommodate the higher current. Following the method just outlined, for an I_{DS} of 19 mA, the gate-source voltage is determined to be V_{GS} - 2.2 V. The remaining resistor values are chosen to establish the desired bias conditions or to provide input or output impedance matching. The dc power consumption for the total circuit is estimated to be 440 mW.

2.2.3 Frequency Response Analysis

The portion of the circuit with the squarewave input should, according to the generally accepted rule of thumb, have a 3 dB bandwidth of five times the squarewave frequency. A 1 Gbps data rate corresponds to a 500 MHz squarewave frequency. Therefore $f_{3\,dB}$ should be ≥2.5 GHz. Assume that at each drive point in the circuit an equivalent RC network (R'C') can be found. Then

$$\tau_r = 2.2\ R'C' = \frac{0.35}{f_{3\,dB}} \tag{2.27}$$

$$R'C' \leq \frac{0.159}{f_{3\,dB}} = 6.36 \times 10^{-11} \text{ sec} \tag{2.28}$$

The FET input circuit can be modeled as shown in Figure 2-5, where R1 is the source impedance (50 ohms), R2 is the matching resistor (50 ohms), and C is equal to

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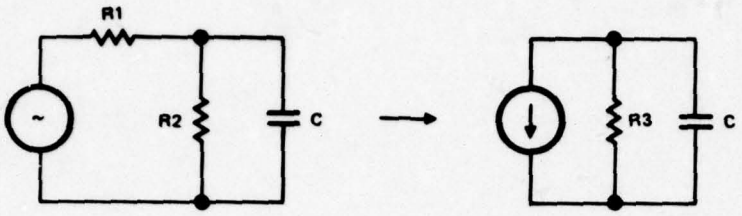

Figure 2-5. Equivalent FET Input Circuit

two FET gate-to-source capacitances in series plus a gate-to-drain capacitance in parallel

$$C = \frac{C_{gs}}{2} + A\,C_{gd} \qquad A = \text{voltage gain} \tag{2.29}$$

In the transformation from a voltage source (left) to a current source (right), R3 is found to be

$$R3 = \frac{R1\ R2}{R1 + R2} = 25 \text{ ohms} \tag{2.30}$$

$$R'C' = 25\,C \quad 6.36 \times 10^{-11} \tag{2.31}$$

$$C \leq 2.54 \times 10^{-12} \tag{2.32}$$

Taking a more reasonable value for C (say 0.5 pF), the 3 dB bandwidth is

$$f_{3\,dB} = \frac{0.159}{25 \times 0.5 \times 10^{-12}} = 12.72 \text{ GHz} \tag{2.33}$$

The FET was designed in the previous section such that its output circuit would have the required frequency response. Actually the FET was somewhat over-designed, as will now be shown. Consider the model of the FET output circuit shown in Figure 2-6. Resistor R_S is the equivalent current source resistance which was implicitly assumed to be infinite in the previous analysis. Although the value of R_S is difficult to estimate, it is expected to be several times larger than R_L, but not infinite. The effect of R_S is to improve the frequency response by the amount the parallel combination of R_S and R_L is smaller than R_L alone

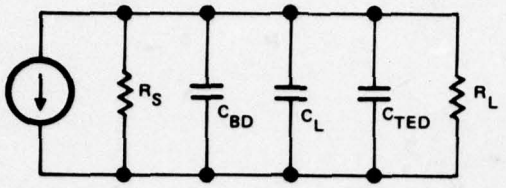

Figure 2-6. FET Output Circuit

$$R' = \frac{R_S\ R_L}{R_S + R_L} < R_L = 1000 \text{ ohms}$$

$$C' = 0.017 \text{ pF} + 0.01 \text{ pF} + 0.03 \text{ pF} - 0.057 \text{ pF}$$

$$R'C' \leq 5.7 \times 10^{-11} \text{ sec}$$

$$f_{3\,dB} \geq 2.79 \text{ GHz}$$

Adequate frequency response of the TED output circuit is assured by making the capacitor large enough so that its reactance at 5 GHz is small compared to 26 ohms. Taking C = 5 pF

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi \times 5 \times 10^9 \times 5 \times 10^{-12}} = 6.36 \text{ ohms}$$

2.3 CIRCUIT DESIGN

2.3.1 Biasing the TED

A typical terminal current-voltage characteristic for the device specified in Section 2.2.1 is shown in Figure 2-7. The operating point is:

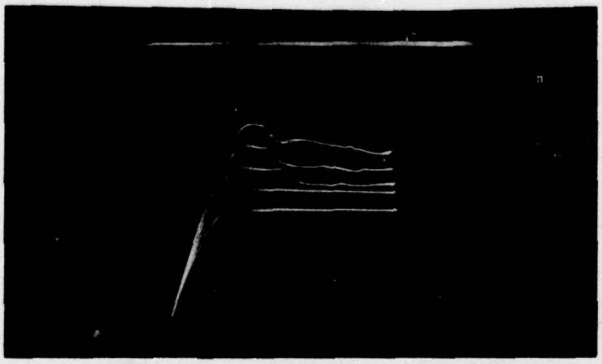

Figure 2-7. Current vs Voltage Curve of the Modulator TED's

V_{AK} = 7.5 volts (anode-cathode voltage)

I_A = 7.0 mA (anode current)

V_{GK} = -4 volts (gate-cathode voltage)

Clearly the device exhibits a differential negative conductance g_d given approximately by

$$g_d = \frac{\Delta I_A}{\Delta V_{AK}} = \frac{6.5 \text{ mA} - 7.3 \text{ mA}}{8 \text{ volts} - 7 \text{ volts}} = -0.7 \text{ m-mhos} \tag{2.34}$$

the differential negative resistance at this point is simply

$$r_d = \frac{1}{g_d} = \frac{1}{-0.7 \text{ m-mhos}} = -1428 \text{ ohms} \tag{2.35}$$

Since outputs of equal amplitude but opposite phase are required from TED's for the applications shown in Figures 2-1 and 2-2, the optimum biasing circuitry is that of symmetrical loads on the cathode and the anode as shown in Figure 2-8. Consequently, the criterion for selecting the values of R1 and R2 is

$$R1 = R2 \tag{2.36}$$

and

$$R1 + R2 < |r_d| \tag{2.37}$$

The selected operating point of the TED device in both applications (modulator and demodulator) is:

$$\begin{aligned} V_{AK} &= 6.5 \text{ volts} \\ I_A &= 6 \text{ mA} \\ V_{G1K} &= V_{G2K} = V_{GK} = -1 \text{ volts} \end{aligned} \tag{2.38}$$

From Figure 2-8, the loop equation can be written as

$$V_S = I_A R1 + V_{AK} + I_A R2 \tag{2.39}$$

From equation (2.39) and condition (2.36) R1 and R2 can be evaluated as

$$R1 = R2 = \frac{V_S - V_{AK}}{2I_A} \tag{2.40}$$

For the modulator case, V_S = 12.5 volts and for the selected operating point specified in (2.38), (2.38) can be evaluated as

$$R1_M = R2_M = \frac{12.5 \text{ volts} - 6.5 \text{ volts}}{2 \text{ (6 mA)}} = 500 \text{ ohms} \tag{2.41}$$

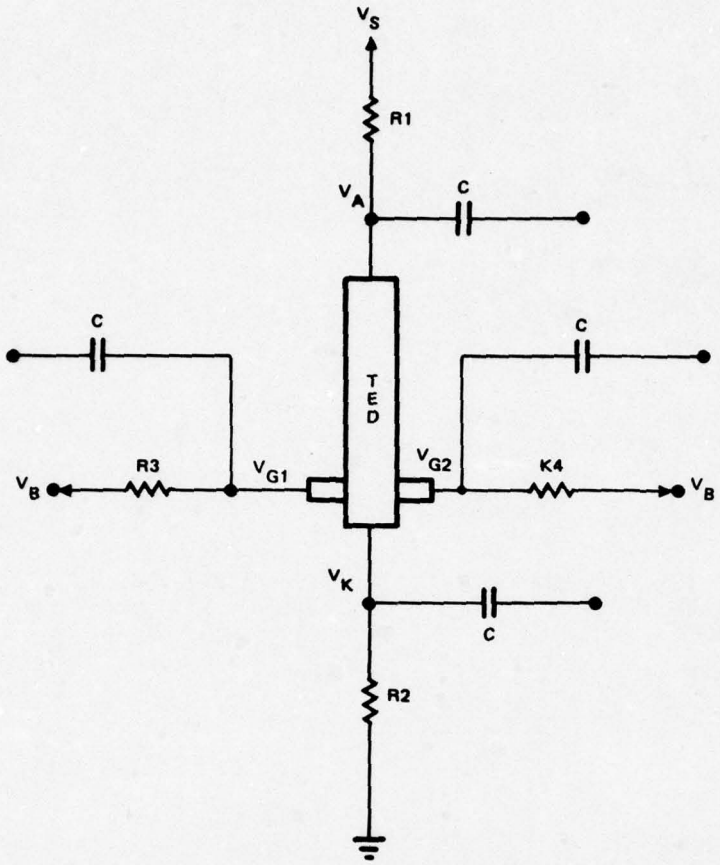

Figure 2-8. Bias Circuitry for Modulator TED's

For the demodulator case, V_S = 10.5 volts. Consequently

$$R1_D = R2_D = \frac{10.5 \text{ volts} - 6.5 \text{ volts}}{2 \text{ (6 mA)}} \tag{2.42}$$

It can be verified that condition (2.37) is being fulfilled for both cases since

$$R1_M + R2_M = 2 \text{ (500 } \Omega\text{)} = 1000 \text{ ohms} < |-1248 \text{ ohms}| \tag{2.43}$$

$$R1_D + R2_D = 2 \text{ (333 } \Omega\text{)} = 666 \text{ ohms} < |-1248 \text{ ohms}| \tag{2.44}$$

For the modulator case, the voltage at the cathode of the TED device is

$$V_{KM} = I_A \cdot R2_M = (6 \text{ mA}) \cdot (500 \text{ ohms}) = 3 \text{ volts} \tag{2.45}$$

For the demodulator, this voltage is

$$V_{KD} = I_A \cdot R2_D = (6 \text{ mA}) \cdot (333 \text{ ohms}) = 2 \text{ volts} \tag{2.46}$$

Consequently in order to have a gate-cathode voltage of -1 volt (as specified by (2.38), the voltages at the gates need to be

$$V_{GM} = V_{GK} + V_{KM} = -1 + 3 = 2 \text{ volts} \tag{2.47}$$

and

$$V_{GD} = V_{GK} + V_{KD} = -1 + 2 = 1 \text{ volt} \tag{2.48}$$

Since the gate input to the TED is a Schottky barrier diode, reverse biased, the only current that flows into the gate is the diode's leakage current. Consequently, resistors R3 and R4 of Figure 2-8 can have a large value and transmit the applied bias voltage V_B to the gates without appreciable voltage drop.

The upper-bound limit for R3 and R4 is set by the following constraints:

- Resistors R1 and R2 have already been determined to be 500 or 333 ohms, depending on the application as specified by equations (2.41) and (2.42). Good design practice for bulk resistors requires that values be within 3 orders of magnitude of each other
- Since resistance is directly proportional to length, a large resistor value requires a large area which is an undesirable condition
- The equivalent input circuit gate 1, of Figure 2-8, is shown in Figure 2-9 where typical values for the device being used are:

$$C_{SB} = 0.01 \text{ pF}$$

$$R_{LEAK} = 100K$$

$$R_{CH1} = 50 \text{ ohms}$$

$$R_{CH2} = 500$$

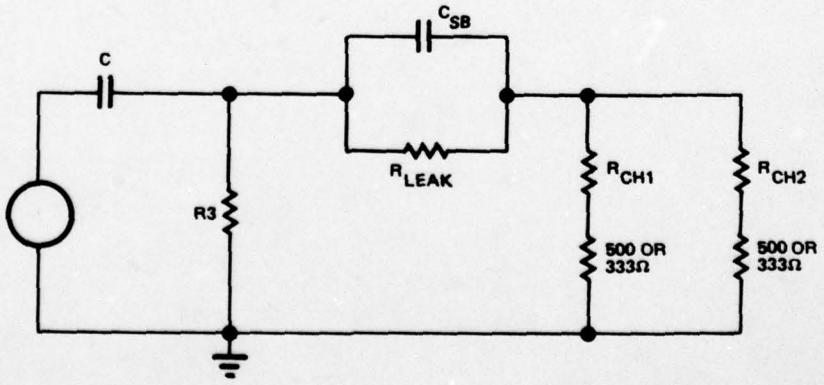

Figure 2-9. Equivalent Input Circuit to the Mod and Demod

The circuit of Figure 2-9 can be further reduced to that of Figure 2-10 by neglecting the reactance of C (coupling capacitor) and assuming $R_{LEAK} \rightarrow \infty$ where

$$Req = (R_{CH1} + 500\ \Omega)||(R_{CH2} + 500\ \Omega) = 354.84\ \text{ohms} \tag{2.49}$$

for the modulator case and

$$Req = (R_{CH1} + 333\ \Omega)||(R_{CH2} + 333\ \Omega) = 262.37\ \text{ohms} \tag{2.50}$$

for the demodulator case. Since it is desired that all the time constants due to external circuitry be smaller than the period of the device signal, the following relationship can be established

$$f < \frac{2.2}{R3\ C_{SB}} \tag{2.51}$$

or

$$R3 < \frac{2.2}{f\ C_{SB}} = \frac{2.2}{(5\ \text{GHz}) \cdot (0.01\ \text{pF})} = 44\text{K} \tag{2.52}$$

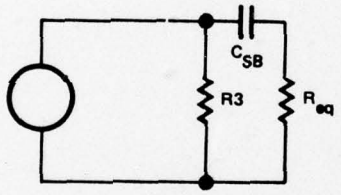

Figure 2-10. Simplified Input Circuit

On the basis of these results, 5.0K was chosen as the value of the gate bias resistors for the demodulator. For the modulator, the drain load resistors were chosen to be 1.0K on the basis of the frequency response analysis of Section 2.3.3. Since the input to the gates of the TED presents approximately a 100K load at low frequencies (modulating signal), this does not affect the performance of the differential stage. Finally, since 5 pF was selected as the value of the coupling capacitor in Section 2.3.3, the same value was used in the demodulator circuit to minimize the design effort.

3. INTEGRATED CIRCUIT LAYOUT

The BPSK modulator and demodulator circuits are shown schematically in Figure 3-1 and Figure 3-3. The layouts of those circuits are shown in Figures 3-2 and 3-4. The topological design of the circuits used a rationale for the layout which included: simplicity, minimum parasitics, minimum area for high yield, and uniform FET and TED gate orientation for ease of alignment. Test devices are also included, such as active devices, Schottky diodes for C-V evaluation of the material, contact resistance bars, and isolated capacitors.

Parallel lines were minimized. Critical lines were separated as far as possible to minimize capacitance between the lines to avoid crosstalk. The high frequency lines were bounded by ground planes forming coplanar lines of a specific configuration. The ground plane lines were separated from the center conductor by 1/2 the width of the center conductor and each ground plane was five times the width of the center conductor. The center conductor was 2 mils wide to facilitate bonding to the center strip with 1 mil spacing on either side. The ground planes were 10 mils wide, which uses up considerable GaAs chip area. Whenever possible, the ground planes were made near the edge of the chip so a portion of the width of one of the ground planes could extend off the chip onto the ceramic substrates. This was not always possible since it was necessary to maintain electrical symmetry in many cases. See Figure 3-2.

Minimizing the chip area was a key consideration in the circuit layout to provide for high yield. Since bonding pads were 3 x 4 mils minimum, the number of bonding pads was kept down by employing a power bus for circuits using the same voltage. The device

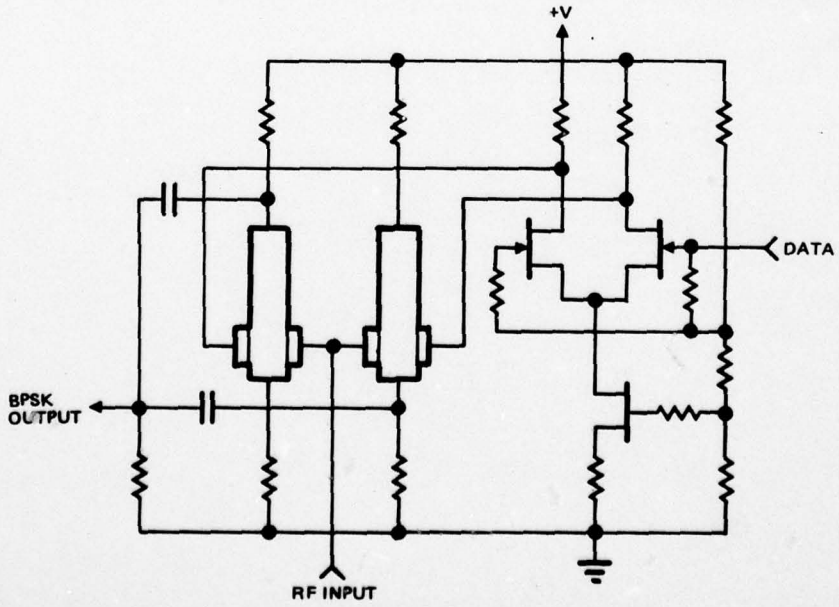

Figure 3-1. GaAs BPSK Modulator

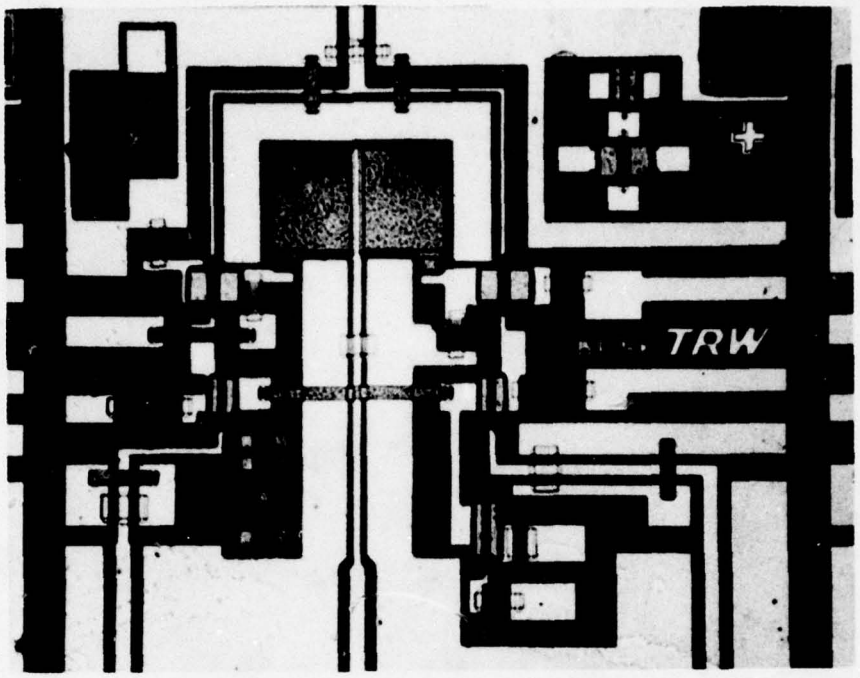

Figure 3-2. BPSK Modulator Layout

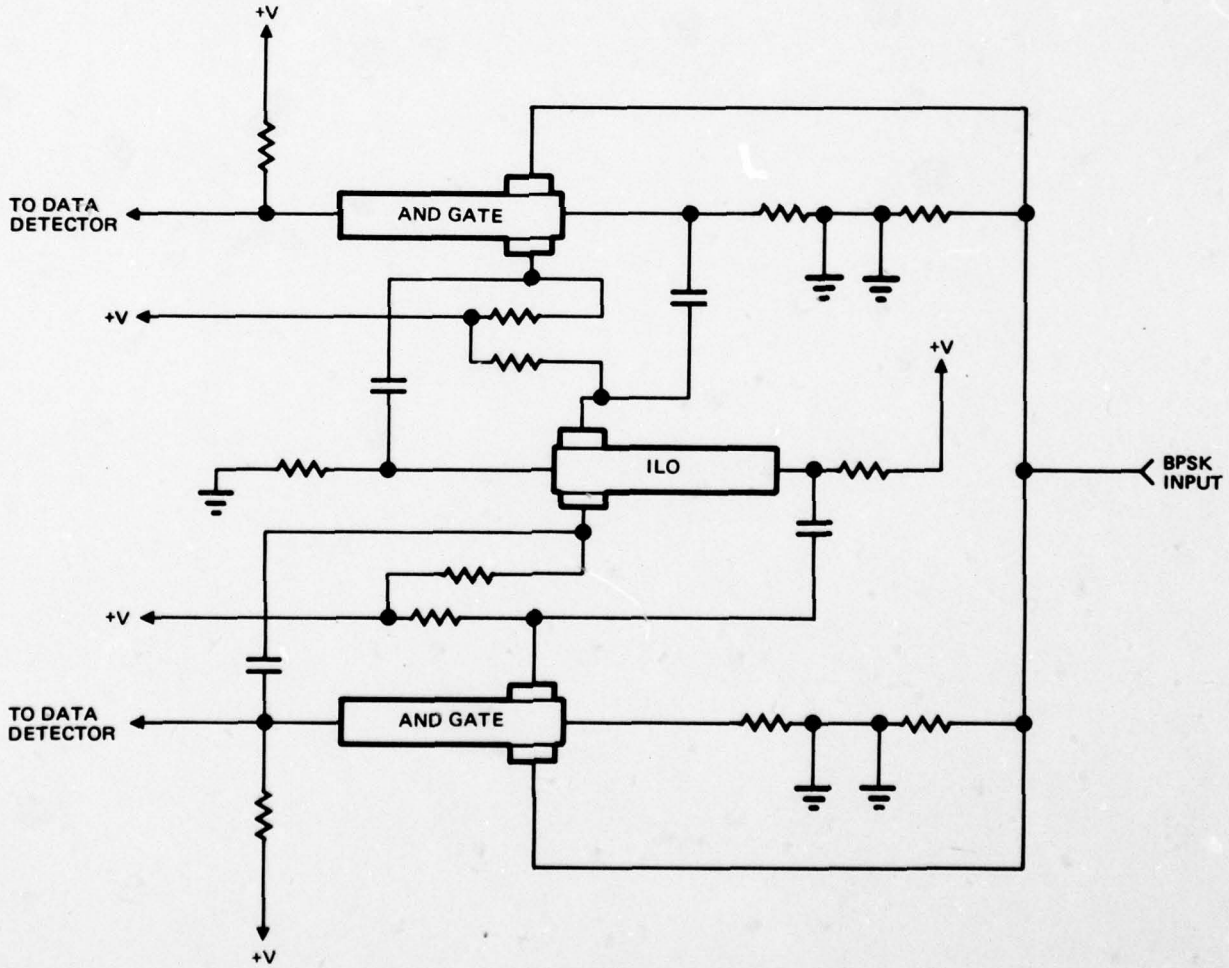

Figure 3-3. GaAs BPSK Demoduator

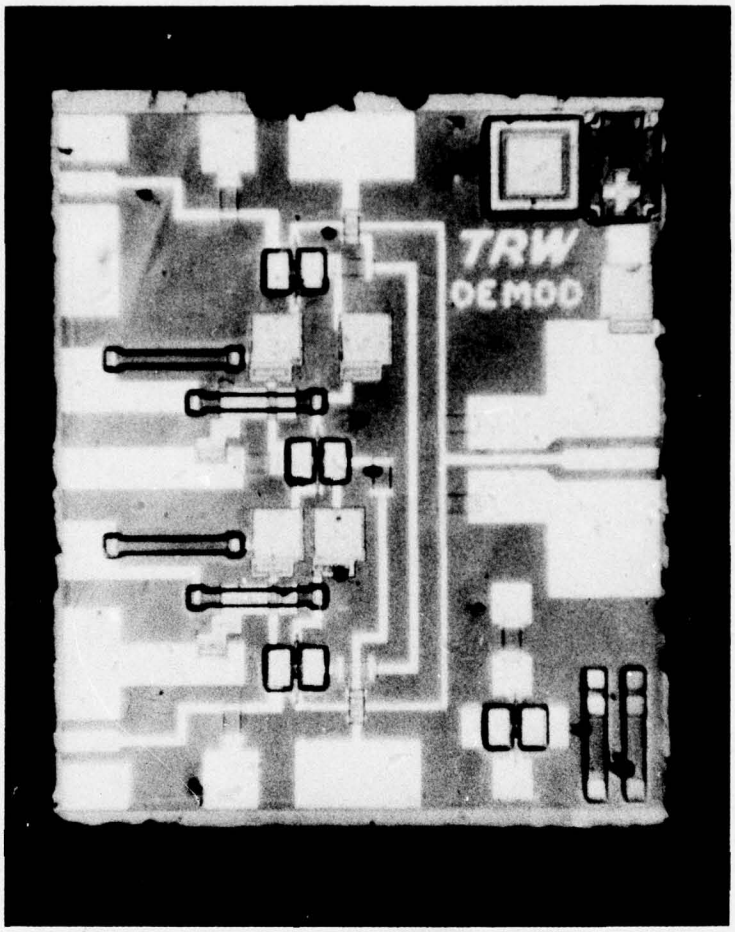

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Figure 3-4. BPSK Demodulator Layout

location did not affect the chip area significantly in that the active devices were small compared to the bonding pads and passive elements. But we wished to locate the devices in a given area and fit the passive elements around the active devices. This was based on the need to have devices very near their neighbors, and the gates oriented to accommodate the selective mesa etching.

The largest passive elements on the wafers were the capacitors. The size of the capacitors used in these circuits was larger than necessary but provided for two methods of fabrication. Crossunders were provided on these circuits to separate high frequency components of the circuit and yet maintain a monolithic design of minimum area. A different layout could have been provided to avoid crossunders; however, it was felt that good isolation could be achieved between the crossing lines using the proposed crossunder technique and the use of crossunders was necessary for future IC's.

The test devices placed on the chips permitted characterization and testing of the devices without circuit parasitics or damage to the circuits. A pattern of resistor bars was placed on each chip to allow for calculating contact resistance.

The contact resistance is calculated from measurements of the resistance on each segment of the resistor bars as shown in Figure 3-5. There are three identical pads with identical contact resistance R_C on the resistor bars. These are separated by a distance, ℓ_s, of 15 μm between pads 1 and 2 and an ℓ_ℓ of 150 μm between pads 2 and 3. The resistance between pads 1 and 2 is called R_s, while the resistance between pads 2 and 3 is called R_ℓ. The contact resistance may be derived as follows

$$R_\ell \text{ (measured)} = R_\ell + 2\,R_C \tag{3.1}$$

$$R_s \text{ (measured)} = R_s + 2\,R_C \tag{3.2}$$

Subtracting equation (3.2) from (3.1) gives

$$R_\ell(\text{measured}) - R_s \text{ (measured)} = R_\ell - R_s \tag{3.3}$$

The ND product can also be derived using the relations

$$R_\ell = \frac{\rho\,\ell_\ell}{WD} \quad \text{and} \quad R_s = \frac{\rho\,\ell_s}{WD} \tag{3.4}$$

where ρ is the resistivity, W the width of the resistor, and D the epi layer thickness.

$$\frac{\rho}{WD}(\ell_\ell - \ell_s) = R_\ell \text{ (measured)} - R_s \text{ (measured)} \tag{3.5}$$

Since $\rho = 1/Nq\mu$ where N is the concentration, q the electronic charge is 1.6×10^{-19} coulomb, and μ the mobility

$$ND = \frac{\ell_\ell - \ell_s}{(R_\ell \text{ (measured)} - R_s \text{ (measured)})\,\mu W q} \tag{3.6}$$

This gives an excellent check on the material properties.

The calculated ND value is substituted in equation (3.1) where

$$R_\ell \text{ (measured)} = 2\,R_C + \frac{\ell_\ell}{Nq\,\mu\,WD} \tag{3.7}$$

thus giving the contact resistance as

$$R_C = \frac{\left(R_\ell \text{ (measured)} - \frac{\ell_\ell}{Nq\,\mu\,WD}\right)}{2} \tag{3.8}$$

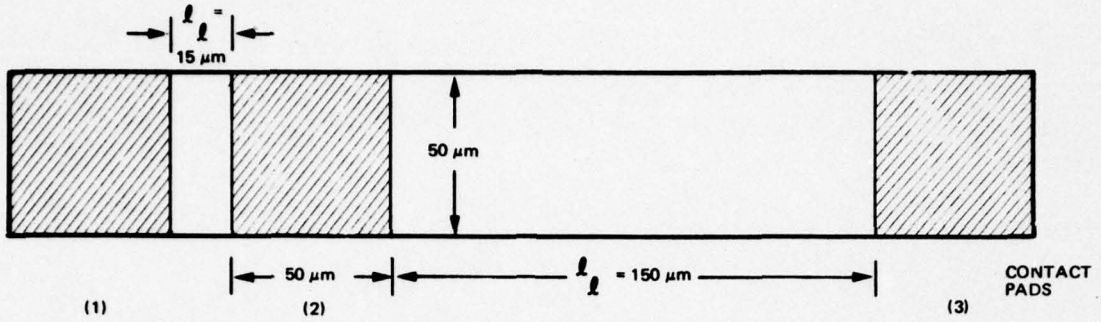


Figure 3-5. Schematic of Resistor Test Bar

4. PROCESS DETAILS AND EVALUATION

4.1 ACTIVE DEVICES

The two types of active devices used in the integrated circuits were FET's and TED's. The primary development efforts were directed toward improving the design criteria and minimizing parasitics to achieve the desired circuit performance. The process development was concentrated in three specific areas: material selection, gate fabrication, and ohmic contacts. This development is discussed in detail in the following sections.

4.1.1 Material Technology

The first circuits processed employed devices fabricated in an active epitaxial layer deposited directly on Cr doped semi-insulating substrates. These layers had an ND = 10^{12} cm^{-2}, with N = 7 x 10^{15} and D = 1.5 x 10^{-4} cm. No differential negative resistance (DNR) was observed with these devices after the gates were applied and only a small DNR was observed before the gates were applied. This was attributed to one of three possible problems: 1) the criteria of ND $\simeq 10^{12}$ cm^{-2} may only be acceptable for certain devices, 2) the interfacial trap density with nonbuffered epi material is too high, or 3) the thickness D is not well characterized.

It was experimentally determined that devices fabricated on epi with ND $\simeq$ 1.5 x 10^{12} would have DNR, while devices fabricated on epi with ND = 1 x 10^{12} would evidence no DNR. At the time the circuits were being fabricated, this was attributed to some uncertainty in the emperical design guide. Analysis carried out more recently shows that the ND = 10^{12} rule is only coincidentally and approximately correct. A better solution would have been to reduce the gate length to less than 1.5 microns. The presence of interfacial traps, and their contribution to the initially observed low DNR, was evidenced both by the light sensitivity of the device current-voltage curves and by pulsed bias testing. Both the traps and the uncertainty in the epi depth measurements were attributed to autodoping and outdiffussion of chrome from the semi-insulating substrates. Both of these problems were obviated by employing a buffer layer between the substrate and the active layer.

The substrates on which the epitaxial layers were deposited were doped with Cr to achieve a resistivity of >10^{6} ohm-cm. These substrates are purchased to a specification of:

- Etch pit density <10^{3} cm^{-3}
- Resistivity >10^{6} ohm-cm
- Surface to be polished to a smooth finish with no visible defects
- Crystal orientation (100) with wafers sliced 3 to 5° off the (100) toward the <110>.

The high resistivity semi-insulating layer was required for device performance while other specifications were made to enhance the surface quality of the epitaxial layers. It is uncertain at this point whether a higher dislocation density significantly affects either the surface of the epitaxial layer or the electrical properties of the devices.

Some earlier investigators have reported a phenomenon in which the surface of the substrates inverts and becomes P-type when the substrates are heated for a period of about 1/2 hour in hydrogen at temperatures greater than 700°C. These conditions are quite similar to the conditions for epitaxial deposition. This inversion has not been observed in our laboratory although precautionary screening techniques were established. However, with this screening it was observed that approximately 10% of one shipment lot of wafers had a high conductivity prior to heat treatment. In the earlier runs when this test was not made we were uncertain as to whether or not the inversion existed. Even if it had existed it would not have been detrimental to our epi process since an in-situ etch is employed prior to epi layer deposition. The primary supplier of Cr doped substrates was Crystal Specialties; the other suppliers could not respond in a time frame acceptable for this program.

The epitaxial deposition technology, although developed in a Company sponsored program, is presented here for continuity. The epitaxial layers are deposited in a vapor phase, vertical deposition system which employs AsH_3, Ga, and HCl as its principal reactants. A schematic of the epitaxial system is shown in Figure 4-1. It consists of a 5-zone furnace, a reactor tube, and a gas flow control system. Zone 1 preheats the entry gases and zone 2 maintains the Ga reservoir at the desired temperature. Zone 4 is the region where epitaxial layer deposition takes place, while zones 3 and 5 are buffer zones for temperature stabilization at zones 2 and 4.

The resistance heated furnace is split and operates with a "clam shell" motion. This aids in rapid cooling of the deposition chamber. The furnace is equipped with heat shields which cover each half of the furnace. These serve to establish an equilibrium temperature in the furnace prior to locking the two halves around the reactor tube, permitting the deposition chamber to be brought rapidly to the desired deposition temperature. This minimizes outdiffusion of dopants from the substrate during the time the wafer is being brought up to the deposition temperature.

The reaction tube has three entry ports for introducing the reaction gases. One port contains the Ga reservoir, through which HCl is passed to form $GaCl_3$. A second port is used for AsH_3 and H_2, and the third port is used for HCl and H_2 for etching and control of the background doping concentration. The deposited layers may be doped with sulfur by introducing H_2S at the second port.

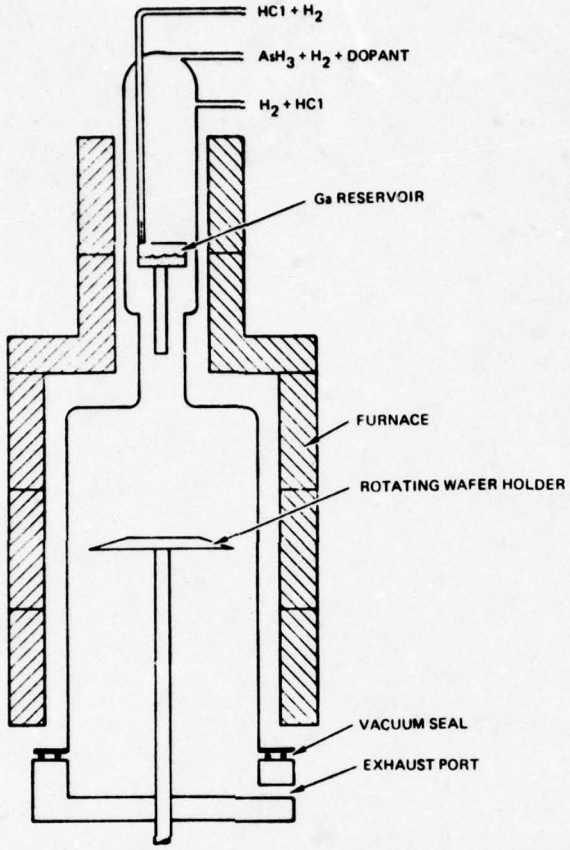


Figure 4-1. Schematic of EPI Reactor

By employing a high concentration of HCl in the reactor gases to reduce incorporation of silicon in the epitaxial layer, buffer layers of GaAs have been grown consistently at less than 10^{13} atoms cm^{-3} impurity concentration. Doped epitaxial films with free carrier concentrations ranging from 10^{15} - 2 x 10^{17} cm^{-3} have been prepared for different applications. For this program, the semi-insulating buffer layer and an active layer with a doping concentration of 1 x 10^{16} atoms cm^{-3} were used.

Results of mobility measurements on epitaxial GaAs layers grown with and without buffer layers are compared in Figure 4-2. The reduction in compensation factor δ when a buffer layer is employed is apparent. As the program progressed, the major changes in the epitaxial material processing sequence were the addition of a buffer layer and a change in the ND product.

The concentration and depth of the active layers were measured and verified by several methods. The depth was measured by a groove and chemical stain technique from a plot of N and D, calculated from C-V data, and measured as a product with N in the resistor test bars. The groove and chemical staining technique for measuring the active layers correlates well with other measurement techniques if a buffer layer is used between the substrate and active layer. Without the buffer layer the depth measured by the two techniques may vary as much as 75%. This variation is related to the

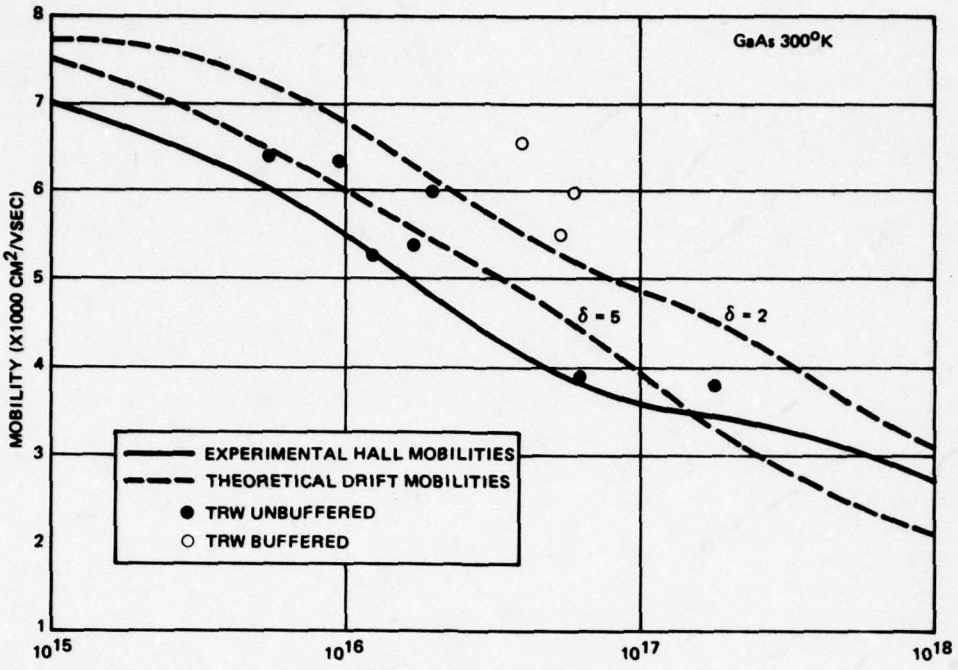


Figure 4-2. Mobility Measurements on Epitaxial Gas Layers

inability to stain and measure the N+/N layer accurately when the transition region is large. The varying width of the transition region may be attributed to several conditions which include variations in Cr in the substrates and variation in the epi growth parameters. The cause of the transition region variation was not studied but the width of the region was minimized with the use of a non-doped semi-insulating buffer layer. Determination of the D and N from C-V data was accurate with active layers on buffers as long as the voltage applied to the Schottky evaluation diode did not exceed the avalanche breakdown voltage of the Schottky diodes, before the epi depletion had spread to the buffer layer (or the pinchoff voltage was reached). In the capacitance-voltage measurement of a Schottky diode the concentration is expressed as

$$N = \frac{C^3}{A^2 \varepsilon\varepsilon_0 q} \frac{dV}{dC} \qquad (4.1)$$

where the capacitance C is the average of two differential capacitance measurements, ε is the dielectric constant, ε_0 the permittivity of free space, q the electronic charge, and A the diode area.

The variation of the diode capacitance with applied voltage is used to determine the electrical thickness of the epitaxial layer. The depletion spreading is expressed as

$$W = \frac{\varepsilon\varepsilon_0 A}{C} \qquad (4.2)$$

The electrical depth is determined arbitrarily as the point at which the doping concentration is reduced by a factor of 2. The C-V data is computed and plotted automatically on a profiler. A typical N vs D plot is shown in Figure 4-3. Further, the ND product is verified from the N value calculated in the Hall mobility measurements. This value is only used for verification of N and D since the absolute values are dependent upon knowing either N or D accurately from an independent measurement. Materials of several ranges with and without buffer layers between the substrate and epilayers were used for device and circuit fabrication. These wafers and their epitaxial lot description are given in Table 4-1.

4.1.2 Mesa and Gate Fabrication

The first step of a planned sequence after epitaxial deposition is device isolation. The device isolation in these circuits is accomplished by mesa etch. The mesas are etched in a solution of H_2SO_4: H_2O_2: H_2O in the ratios of 5:1:1 at room temperature at a rate of 2 μm per minute. It was observed that GaAs material grown on the (100) direction exhibits preferential etching of the (111) planes in the above etchant. The resultant mesa profiles are shown in Figure 4-4.

Photolithographic patterns are used to delineate the mesas during this isolation etch. This pattern must be aligned to the proper plane $<01\bar{1}>$ to ascertain that the gate metal will cover the mesa with a gradual slope. A typical mesa showing good gate coverage is shown in Figure 4-5. The depth of etch must be sufficient to go through all of the active layer and approximately 0.5 to 1 μm through the buffer layer to assure device isolation.

Gates are applied to the mesa in the next major step of the process sequence. Gate fabrication prior to ohmic contact deposition in the process sequence was selected to enhance alignment capability of narrow geometries. It was observed on other contractual work that this sequence, with the present metallization system, gave a reduced yield in the capacitors; therefore, this sequence was subsequently changed.

DISTANCE FROM JN (MICRONS)	CARRIER CONCENTRATION (CM^{-3})	10^{15}	10^{16}	10^{17}	10^{18}
0.202	2.941E + 16				
0.214	2.361E + 16				
0.228	2.529E + 16				
0.242	2.403E + 16				
0.259	2.415E + 16				
0.280	2.391E + 16				
0.303	2.115E + 16				
0.342	1.688E + 16				
0.397	8.679E + 15				
0.458	3.612E + 15				
0.538	1.492E + 15				
0.650	6.928E + 14				
0.823	3.138E + 14				
1.045	1.417E + 14				
1.459	6.694E + 13				
2.548	1.772E + 13				
4.787	4.899E + 12				

Figure 4-3. Computer Printout of Concentration vs Depth of an Active Layer on a Buffered Epitaxial Layer

Table 4-1. Detail of Various Lots

Modulator					
Number	Epi	Concentration	x_j (μ)	Buffer Y/N	Disposition*
1	606	7×10^{15}	0.8	N	(1)
2	610	2×10^{16}	1.0	Y	(1)
3	671		1.5 to 2.0	N	(1)
4	364	1.9×10^{16}	3.0	Y	(2)
5	482	0.8 to 1×10^{16}	1.9	N	(2)
6	791B	5×10^{15}	1.9	Y	(2)
7A	877A	6×10^{15}	1.65	Y	(2)
8A	920	1.1×10^{16}	2.7	N	(2)
9A	921	1.1×10^{16}	4.2		(2)
10	912B	1.1×10^{16}	1.75	N	(2)
11	974	1.8×10^{16}	4.0	N	(3)
12	1006	3×10^{16}	1.05	Y	(3)
13	1006	3×10^{16}	1.05	Y	(4)
14	1042	2×10^{16}	0.9	Y	(3)
15	1006	3×10^{16}	1.05	Y	(6)
16	1042	2×10^{16}	0.9	Y	(6)
17	1006	3×10^{16}	1.05	Y	(6)
18	1045	2×10^{16}	0.6	Y	(5)
19	1047	1.6×10^{16}	0.8 to 1.1	Y	(5)(3)
20	813	3×10^{16}	0.5	Y	(5)(3)
21	815A	5×10^{16}	0.63	Y	(5)(3)
22	813	3×10^{16}	0.5	Y	(5)(4)
23	812	4×10^{16}	0.5	Y	(5)(4)

Table 4-1. Detail of Various Lots (Continued)

Demodulator					
Number	Epi	Concentration	x_j (μ)	Buffer Y/N	Disposition*
1	765	1×10^{16}	1.5	Y	(2)
2	783	1.5×10^{16}	1.5	N	(2)
3	675	1×10^{16}	0.84	Y	(2)
4	872	5×10^{15}	2.25	Y	(2)
5	879A	1×10^{16}	1.0	N	(2)
6	919	9×10^{15}	4.3	N	(2)
7	920	1.1×10^{16}	2.7	N	(2)
8	921	1.1×10^{16}	4.2	N	(2)
9	912B	1.1×10^{16}	1.75	N	(2)
10	974	1.8×10^{16}	4.0	N	(2)
11	816	4×10^{16}	0.6	Y	(3)
12	921	1.1×10^{16}	4.2	N	(3)
13	1006	3×10^{16}	1.05	Y	(4)
14	1047	1.6×10^{16}	—	Y	(4)

*Modulator and Demodulator Wafer Parameters and Wafer Lot Disposition:

(1) Wafer lot used to evaluate processing techniques.
(2) Standard MOD-1 process, poor peak-to-valley ratio/FETS reasonable.
(3) Poor capacitor yield.
(4) Good circuits to assembly.
(5) Evaluated MOD-II process.
(6) Evaluated thinning techniques.

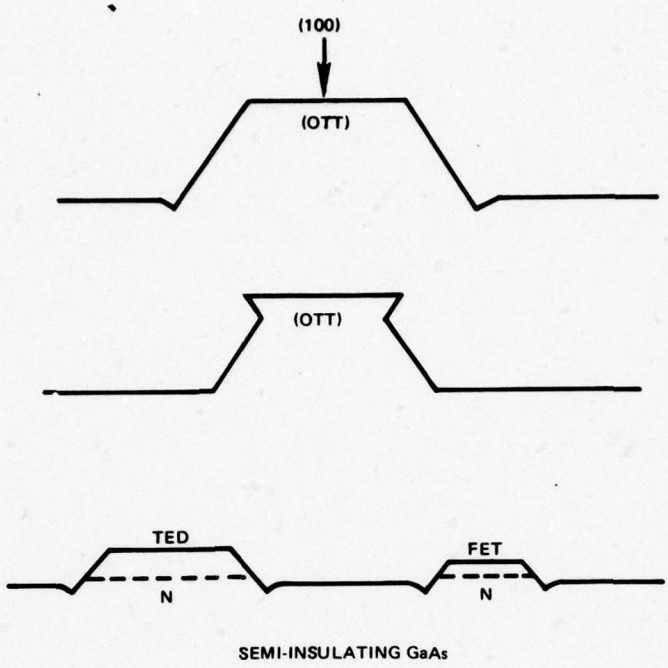


Figure 4-4. Mesa Profile

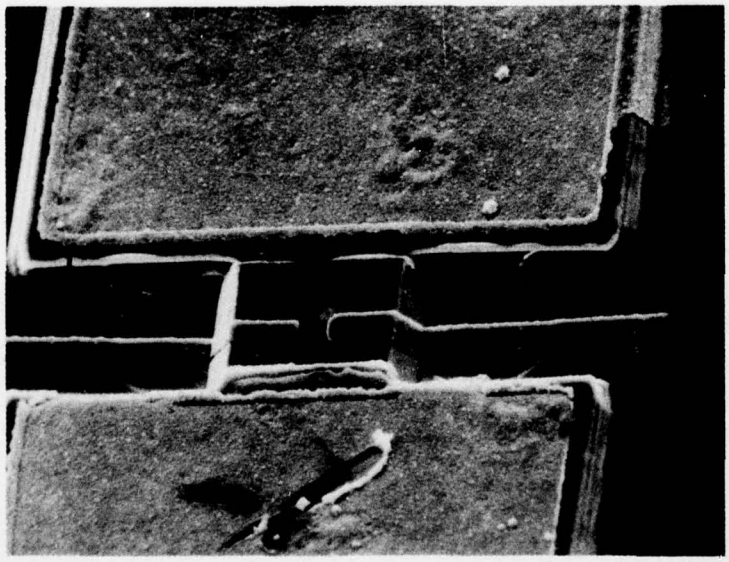


Figure 4-5. Typical Mesa Showing Good Gate Coverage

There was no preferred technique for forming the Schottky gates in that Schottky barriers by either technique gave sharp, low leakage device characteristics. The quality of the diodes was clearly a function of the cleaning technique and post deposition sinter conditions. A light clean of the gate region with a peroxide-ammonia oxide etchant and a sinter of about 10 minutes at 300°C was sufficient to achieve the good diode characteristics.

4.1.3 Ohmic Contact Development

Ohmic contacts to GaAs have been extensively studied at TRW and in other laboratories. The objective of these studies was to achieve metal semiconductor contacts which exhibit linear current-voltage characteristics and a contact resistance low in comparison to the resistance of the semiconductor device. This, in principle, is achieved either by:

- The choice of a metal which forms a low barrier with the semiconductor (thermionic emission)
- A high concentration region in the semiconductor near the contact so that the barrier is readily penetrated by quantum mechanic tunneling.

The tunneling approach was taken for the GaAs materials. In general, the objective was to reduce the specific contact resistance, γ_c, to about 10^{-5} ohms-cm^2 by doping the semiconductor. This has been demonstrated in TRW's TED devices and in these circuits.

The low specific contact resistance was achieved by doping the GaAs with Ge from a AuGe contact. The Ge, an amphoteric dopant, goes substitutionally on vacant Ga sites to form donors. The doping occurs as the Au and Ge alloys with the topmost layer of the GaAs. When the GaAs-AuGe alloy solidifies, Ge is distributed in the GaAs regrowth layer. Contacts formed in this manner yield a low ($\approx 10^{-5}$ ohm-cm^2) specific contact resistance.

The basic AuGe contact metallization has been used with and without variations in the structure. The variations included the use of additives such as silver, indium, platinum, and nichrome to reduce the surface tension and minimize "balling" in the contact areas. For many of the early TED devices and the early circuit development, the AuGe contact was used with simply a coating of Au for bonding purposes. These contacts were not uniform throughout the contact area or across the wafer but had many islands of contact metal in the ohmic contact region. This caused the ohmic contact resistance to be higher than that achievable with a more uniform contact.

The nonuniformity was, in part, attributed to cleanliness of the wafer prior to metal deposition and to localized segregation of metal clusters due to the high surface tension of the metal. A cleaning technique which removed surface oxides was developed and employed during the circuit fabrication. This technique uses either dilute HCl or dilute NH_4OH to remove the oxides. The new cleaning procedure gave a higher yield of

good contacts across a given wafer but the balling still existed. Balling was eliminated with the use of our present metal configuration and different sintering conditions.

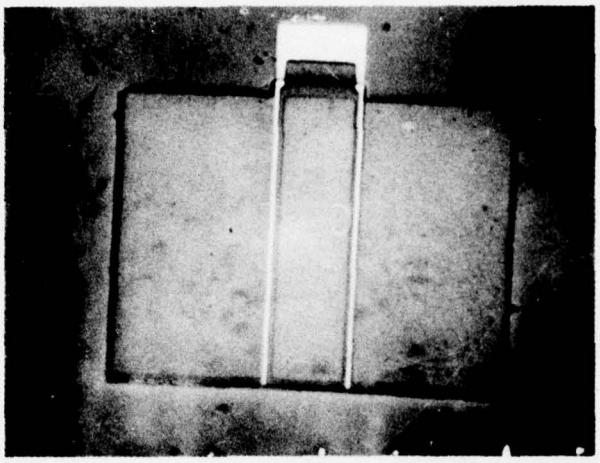
Metals with various thicknesses of Au, Ge, Au (top metal), and Ni or Pt were investigated. The system of AuGe PtAu Pt was employed in the monolithic circuits developed on this program. Platinum was chosen over Ni because Ni contacts gave a high contact resistance, was a more difficult process, and exhibited some deterioration with age. The thickness of the metals used in the ohmic contact were: Ge, 200 Å; Au, 300 Å; Pt, 400 Å; and Au, 3000 Å; Pt, 400 Å. These contacts were deposited either by vac-ion evaporation or RF sputtering. It had been shown earlier that an optimum sinter temperature and time for the AuGe contacts was 450°C to 500°C for 2 to 5 minutes. Temperatures exceeding 500°C and times exceeding 5 minutes caused an increase in the specific contact resistance. Typical values of specific contact resistances achieved with this metallization system was on the order of 10^{-5} Ω-cm^2.

A comparison of the AuGe Au contact and the AuGe Pt is shown in Figure 4-6. It is clear that the ohmic contact balling is alleviated with the use of the Pt overlay. Although these were experimental circuits it was felt that the Pt layer represented an excellent barrier between the AuGe contact and the topmost Ti-Al interconnect metal for future contact reliability.

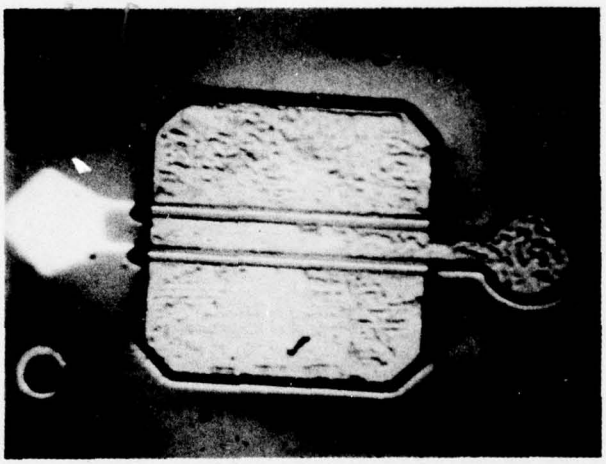
The ohmic contacts were generally deposited after the aluminum gates had been formed to facilitate good gate alignment. It was planned that chromium photolithography mask would have been used and the view of the contact pads would have been improved. However, iron oxide masks were used, and either sequence was acceptable from an alignment viewpoint. The gate deposited first sequence was thought to be compatible with the other processing steps since the aluminum gates could withstand temperatures up to 500°C without any appreciable degradation. Further, the upper limit on the time and temperature at which the ohmic contacts could be exposed and still exhibit a low contact resistance was already established. This sequence later proved to give a lower circuit yield than when the gates were deposited and sintered after the ohmic contracts had been formed. The decrease in yield with the former technique was caused by deterioration in capacitors processed in that manner. Details of the process yield are discussed in Section 4.3.

4.2 PASSIVE DEVICES

The passive elements in the integrated circuits include thin film capacitors, bulk and thin film resistors, undercrossings, and interconnect metallization. The capacitor was processed as planned in the proposed process sequence but subsequently developed more extensively under the ONR A/D contract. The bottom plate of the capacitor is Al, deposited in the same definition as the Al gates and crossunder metal. The dielectric for the MOM capacitor was formed by masking with photoresist to reveal the capacitor and undercrossing areas and then anodizing using an aqueous 3% tartaric acid solution.



a) With Platinum Overlay



b) Without Platinum Overlay

Figure 4-6. Comparison of AuGe Contacts

The depth of anodization was ≈1500 Å with about 3500 Å of metal left after anodization. The top plate of the capacitor is TiAl formed in the deposition of the interconnect metal. A significant development effort was required to achieve the desired parameters for the thin film resistors and to achieve acceptable interconnect metallization. This development effort, which resulted in a high device and circuit yield, is described below.

4.2.1 Resistors

Thin film resistors were used in the modulator circuit and both thin film and bulk resistors were used in the demodulator circuit. The thin film resistors were used in applications which required a small value of resistance with high precision. The bulk resistors were employed in circuit applications where the resistance value was several thousand ohms and noncritical. The resistance values in the basic modulation circuits varied from 50 to 1000 ohms. Therefore, a resistor material with a sheet resistance of 200 ohms/□ was chosen for minimum resistor area and ease of processing.

Several materials were considered as candidates for fabricating resistors. These included nichrome, cermet, and CrGe. The chromium germanium material was chosen since it was the most stable of the materials, was compatible with GaAs processing, and easily used in achieving the target resistor values. The nichrome required large area resistors and it was difficult to form a low resistance contact on the material after oxidation and other heat treatments. An equimolar mixture of CrGe was used in the resistors to give a resistance of 1000 μohm-cm. During heating, the resistance rises, but in a predictable manner. The contact resistance of this material is unaffected by low temperature oxide deposition. Low resistance contacts have been successfully made to this material with the TiAl interconnect metal.

After the material was selected and the deposition condition established, a process for delineating the resistors was established. The resistor dimensions are defined using a photoresist and etched in a buffered ferricyanide solution, which was developed specifically for the GaAs circuit.

Several methods of depositing the resistor were tried. These included E-beam evaporation, resistance heated boats, RF sputter deposition, and a resistance heated crucible. The vapor pressure curves of chromium and germanium intersect at approximately 1300°C. Therefore, if this temperature can be maintained throughout the evaporation run, the composition of the vapor and the melt will remain constant. Since previous work had indicated that the equimolar mixture would have a resistivity of 1000 μohm-cm, we started with this composition and tried to maintain a constant temperature of 1300°C. A glass bar 10 squares long was inserted into the chamber to monitor the resistance during the run. The wafer temperature was also monitored, but this proved to be an uncontrollable variable since radiant heaters were only available in the load-lock area and the block heater in the wafer holder heated each wafer differently depending on the contact area.

Depositions using the E-beam gun were made while trying to follow a particular resistance vs time curve which had been found to give a good result. However, since the beam was not swept and the crucible in our system was very small, it was difficult to avoid hot spots in the melt. This caused an excess of chromium to be deposited even

if the resistance was on target. Subsequent heat treatments had different and unpredictable effects on the resistivity depending on the actual resistor composition. The wafer and monitor bar resistances also differed so this method of deposition was abandoned.

Resistance heating was tried using molybdenum, tantalum alumina coated boats, and finally tungsten boats. It was difficult to repeat constant temperature runs on any of the boats and in many cases the liquid melted through the boats, even the alumina coated boats. This susceptibility to run abortion at unknown times was undesirable. The tungsten boats appeared to give the most reproducible results but only when the deposit was 500 $\mu\Omega$-cm and at least 500 Å thick. This meant that the sheet resistance was 100 $\Omega/\square$, half of the value used in designing the circuits. Thinner, high sheet resistance deposits were very temperature sensitive. Since none of these runs gave predictable, reproducible results, this method of evaporation was also abandoned.

Concurrent runs were made in a sputtering system using a mixed chromium germanium target. This deposit acted differently from the evaporated mixture in that it did not etch in the same etch solution and had to be sputter etched. During temperature stabilization, the deposit also caused the underlying low temperature oxide to blister which left holes in the resistors. This effect was eliminated by using a sputtered oxide underneath the resistors, but the method still did not yield reproducible results. One IC run was made using this technique, but the resistance did not rise significantly during high temperature stabilization as anticipated from prior practice runs. Therefore, this resistor deposition method was abandoned.

At this time an evaporation "furnace" was installed in the evaporator. This consists of a resistance heated alumina crucible with appropriate reflective shielding. There is a spring loaded thermocouple touching the bottom of the crucible to monitor the temperature. Initial runs were made while heating the substrates. This resulted in unpredictable resistivity variations between the glass monitor bar and the gallium arsenide wafers. This effect has been essentially eliminated by allowing the preheated wafers to cool to 60 to 70°C prior to the evaporation. The monitor bar and the wafers now agree within 10%, and the resistivity rises 200 to 225% during stabilization at 475°C.

4.2.2 Interconnects and Isolation Techniques

Most of the circuit elements are joined by the top metal; however, both circuits require some connections through undercrossings in order to minimize the area and maintain a symmetrical layout. These connections are made with aluminum conductors which are deposited and defined along with the capacitor plate and gates. After this they are treated as one entity because they all must be protected by a deposited oxide and a hole must be etched into this oxide to permit contact to the top metal. This oxide

also prevents the aluminum from reacting with the ohmic contact metals, particularly gold, and with the etches, some of which attack aluminum. The oxide is deposited by the oxidation of silane at 390°C. An RF sputter deposit could also be used if the system did not get excessively hot.

Titanium-aluminum was chosen for the top metal because aluminum is easily bonded and etched while the titanium makes low resistance contacts to the resistors, bottom aluminum plates, gates, and the platinum on the ohmic contacts. The metal must be sputter deposited rather than evaporated in order to assure the low contact resistance required to the bottom aluminum. However, sputtered metal on oxide-coated GaAs wafers is often under such great stress that it rips holes in the oxide when the metal is removed during etching. Bias sputter deposition, that is sputtering with a small negative bias on the substrate, reduces this stress. In addition, close control of the etch rate and temperature has minimized this effect. The resultant metal stripes are adherent to the oxide, but the metal is still sintered at 300°C to reduce the contact resistance to the underlying metals.

Following final test the chips are separated by scribing and/or sawing. The sawing results in a ragged edge which is particularly bad in the $[0\bar{1}\bar{1}]$ direction. Therefore, this direction is usually scribed and broken. However, when it is desirable to have metal ground planes, for example as close to the edge of the chip as possible, then the wafer has to be sawed. This can only be done in the "good" $[01\bar{1}]$ direction where the minor chipping of the GaAs does not remove top metal.

4.3 PROCESS DEVELOPMENT RESULTS

The processes developed and used in the fabrication of the monolithic GaAs BPSK modulator and BPSK demodulator circuits have demonstrated that the mesa technology can be successfully used for small scale integrated circuits. In this technology, active devices which included FET's and TED's and passive elements were fabricated with a high component yield of about 90%. An overall yield for processing the circuits was from 25 to 46% depending on the processing techniques. The major yield problem was in the capacitor fabrication. A yield of about 85% was achieved, whereas a yield of 95% is required for successfully fabricating circuits at a high yield.

4.3.1 Individual Device Results

The primary active components in the circuit were the TED's. These devices were evaluated during processing for peak current to valley current ratio, peak voltage, and contact resistance. The peak-to-valley current ratio was very small — less than 5% for devices fabricated on epi layers with ND = 10^{12} cm^{-3} and without the use of buffer layers. Devices with an ND > 1.5×10^{12} cm^{-3} and buffer layers gave greater than 10% peak-to-valley current ratios.

Once it was established that the ND value was adequate, the individual TED or FET component yield varied from 85 to 91%. The primary factor in the lower yield was the manner in which the gates were applied to the device. If the gates were applied prior to forming the ohmic contacts (mod process-1), the yield was lower than if the ohmic contacts were formed first (mod process-2). This is attributed to variations in the aluminum metal at the 500°C ohmic contact sintering temperatures. Typical capacitors developed for the modulator and demodulator circuits suffered degradation similar to that of the aluminum gates in that excessive shorting occurred with capacitors fabricated earlier in the processing sequence. This data is compared in Table 4-2. The "TED or FET" column in this table represents the visual and ohmic contact yield. The yield of capacitors processed prior to ohmic contact formation was 72%. Capacitors, when fabricated after the ohmic contacts had been formed, had a yield of 86%. This yield, although adequate for small scale integrated circuits, must be improved for MSI or LSI.

Table 4-2. Typical Component and Circuit Yields (Percent)

Circuit	Capacitors	Gates	TED or FET	Resistor	Circuit Yield	
					Calculated	Actual
Modulator (Mod Process)-1	72	85	99	99	23	22
Modulator (Mod Process)-2	86	91	99	99	41	35
Demodulator	86	91	99	99	21	23

The improvements in circuit yield for MSI and LSI technology can be viewed by considering how the component affects the overall circuit yield. The circuit yield may be expressed as

$$Y_I = Y_E^n$$

where Y_I is the integrated circuit yield, Y_E the discrete element yield, and n is the number of elements in the circuit. With this formula for the modulator and demodulator for the various processes, the yield was statistically predicted as shown in in the circuit yield column in Table 4-2. The slightly higher yield, than calculated, in the case of the modulator circuits, indicates that a cluster of defects in a given area of the wafer may have been responsible for the low capacitor yield.

Considerable effort was expended in developing resistors to meet the circuit design value. Since the resistor values are modified with an initial heat treatment, this had to be considered in the initial resistor target value. A lower resistance value than that required for the circuit was used, and this value changed to the final

Table 4-3. Thin Film Resistor Results

Modulator Lots	Nominal Resistors		
	500 Ω	1000 Ω	50 Ω
Mod 22 (Mod-process-1)	522 ±29	1019 ±44	45 ±2
Mod 16 (Mod-process-2)	498 ±43	969 ±78	51 ±4
Mod 17 (Mod-process-2)	480 ±11	934 ±35	47 ±2

value during the in-process heat treatments. The maximum variation for resistors in the circuits was as high as ±8% and as low as ±2%. The nominal values of the resistors in the circuit did not vary from the target value more than 4%, as shown in Table 4-3.

A comparison of the designed and measured device parameters is given in Table 4-4. The change in ND product for the FET's and TED's from the designed value was required for DNR for the TED's. This change caused the variation in other parameters, such as the I_p and I_{dss} for the TED's and FET's, respectively.

Table 4-4. Design and Measured Device Parameters

Values	Design	Measured
	FET	Mod 23
N	2×10^{16}	4×10^{16}
Nd	1×10^{12}	1.97×10^{12}
g_m	4 mmho	3.5
Idss	18.6/11.2 mA*	33
Values	TED	Mod 23
Nd	1×10^{12}	1.97×10^{12}
V_p	7 V	5.5
I_p	6 mA	7.3

*Thinned.

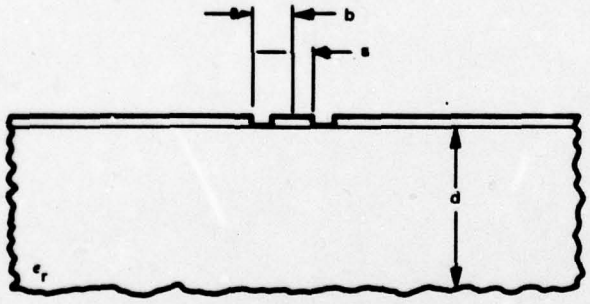
5. TEST AND EVALUATION

5.1 TEST EQUIPMENT

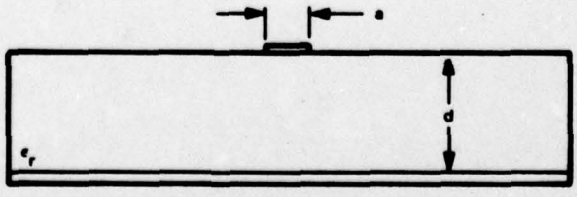
5.1.1 Test Fixtures

Due to the scale of component integration requirements in the BPSK modulator and demodulator circuit designs, new approaches had to be developed in the type of transmission media used to access the IC chip. Coplanar waveguide was determined to be better suited for this task than the previously used microstrip.

Coplanar waveguide consists of a thin strip of plated metal on the surface of a dielectric slab with two plated metal ground planes running parallel to the strip on the same surface, as shown in Figure 5-1. If one assumes that the ground planes are infinitely long and the dielectric material infinitely thick, the characteristic impedance, Z_0, of the line is a function of the ratio a/b and the ϵ_r of the dielectric. This indicates that for a given ϵ_r and a desired Z_0, the size of the center conductor of the coplanar line may be varied on the substrate without changing Z_0 as long as the ratio a/b remains constant. This is in contrast to microstrip where a change in the conductor width causes a change in Z_0. Naturally, an infinitely thick substrate and infinitely long ground planes can only be approximated. When a coplanar waveguide is placed in a container or mounted in a test fixture, the surrounding ground planes of the walls, top, and bottom of the fixture may be used to approximate an infinite ground plane on the substrate. However, the position of these added ground planes relative to the various transmission lines on the substrate may alter the line impedance.



a) COPLANAR WAVEGUIDE



b) MICROSTRIP WAVEGUIDE

Figure 5-1. Comparison of Geometries of Coplanar and Microstrip Waveguides

Investigation into this surrounding ground plane effect shows that the top and bottom ground plane positions effectively lower Z_0 when the planes come close enough to affect the field patterns between the center conductor and the parallel surface ground planes (Figure 5-2). Figure 5-3 demonstrates that as the center conductor is made smaller, the effect of the fixture side walls on Z_0 becomes less.

To assure the position of the bottom ground plane in the fixture and to allow the connection of all the surface grounds for continuity, a bottom ground plane was added to the coplanar substrate design. Figure 5-4 shows the effect the top of the fixture has on Z_0 for a fixed bottom ground plane position. Note that the effect of this ground plane becomes negligible at a point greater than 0.030 inch above the transmission surface.

When more than one transmission line is plated on the dielectric, the isolation between the transmission lines is an important characteristic. The amount of isolation is proportional to the amount of ground plane between the two lines. To achieve a respectable 50 dB of isolation requires a ground plane distance of at least 10 times the width of the center conductor between the two adjacent lines. Since the center conductors used are small, the chip designer can have two or three transmission lines on one side of the IC chip with minimal cross-coupling between the lines. The impedance of the transmission lines used in the modulator and demodulator test fixture is 50 ohms. The center conductor width is 20 mils at the connector interface and 2 mils at the chip/substrate interface.

The use of coplanar waveguide requires the IC chip surface to be in the same horizontal plane as the substrate surface so that the ground plane and center conductor interface with the chip is as continuous as possible. To satisfy this requirement and to simplify the mounting of the IC chip to the test fixture, the modulator and demodulator substrates were made in two L-shaped configurations. The two halves fit together to form a rectangular shaped hole near the center of the substrate. A similarly shaped base was constructed to accommodate the two substrate halves and provide a mounting pedestal for the IC chip and the connectors, as shown in Figure 5-5. The fixture was machined from brass and coated with a copper flash and an emersion gold finish. This design allows the IC chip to be properly aligned with the 2 mil coplanar lines and the surface of one-half of the substrate while it is being epoxied to the fixture. The other side of the chip can then be properly aligned with the other half of the substrate by placing the fixture halves together and adjusting the moveable side of the substrate until the 2 mil transmission lines are correctly aligned. The fixtures can then be bolted together, securing the alignment.

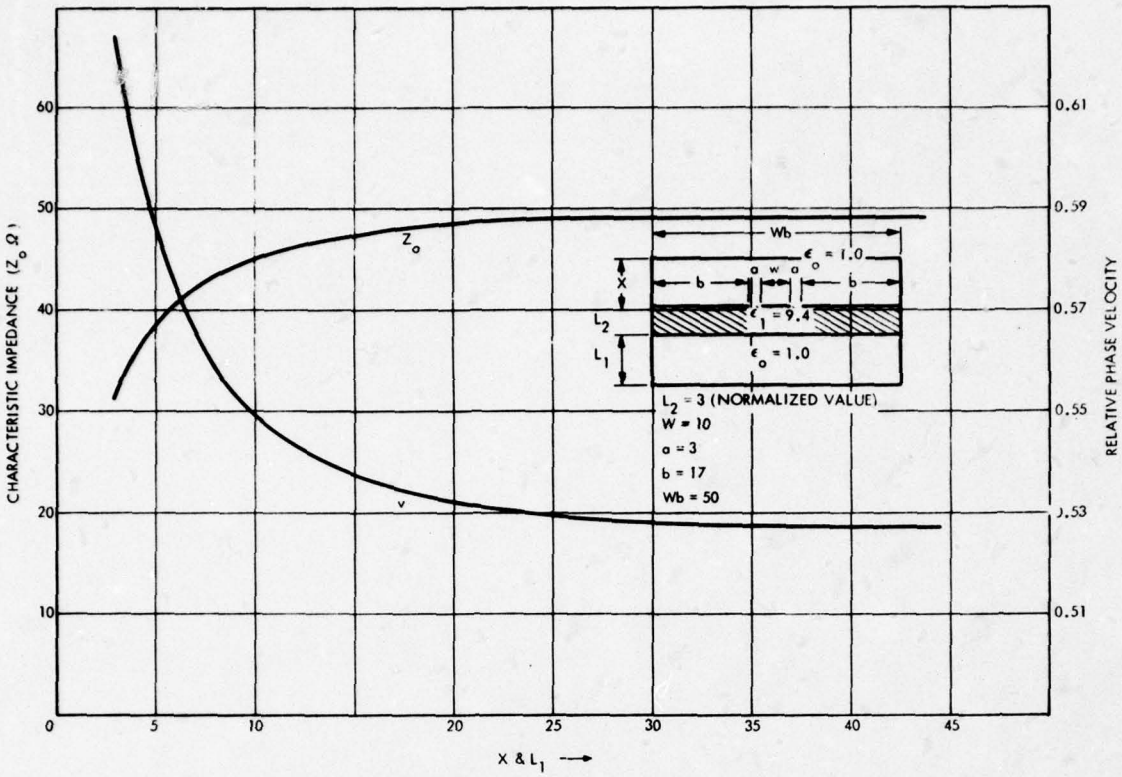


Figure 5-2. Variation in Characteristic Line Impedance and Relative Phase Velocity of a Coplanar Waveguide as a Function of Top-and-Bottom Ground Plane Position

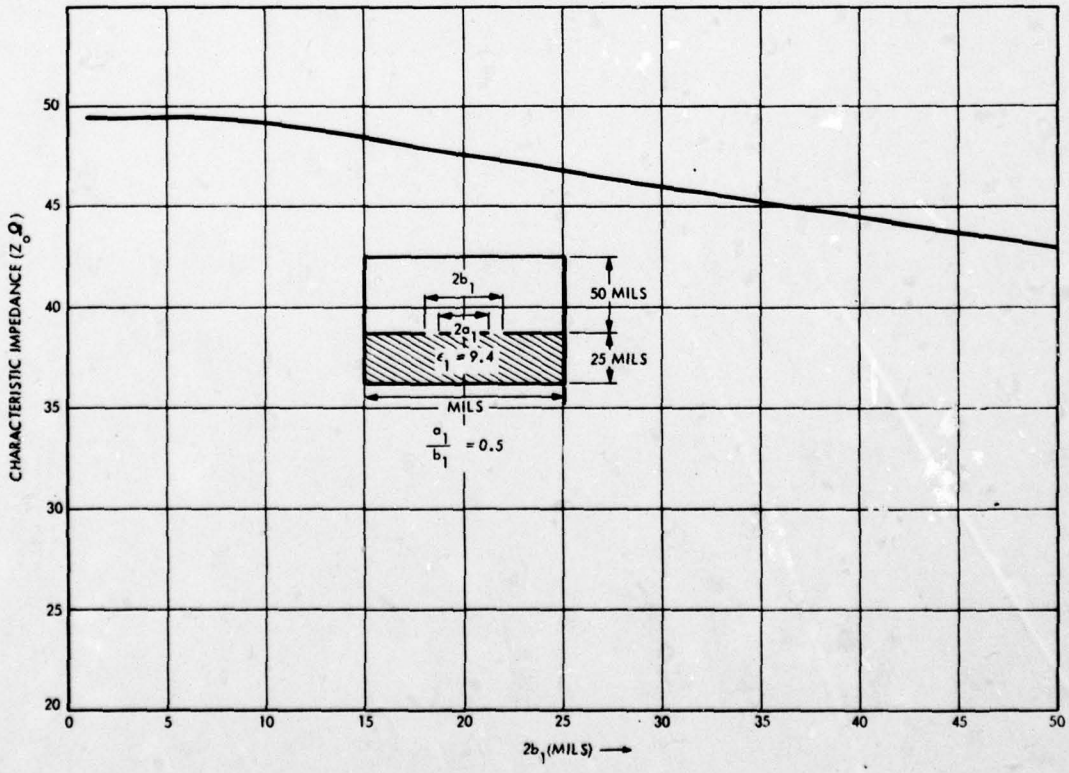


Figure 5-3. Variation in Characteristic Line Impedance of a Coplanar Wave-Guide as a Function of Side Wall Ground Plane Spacing

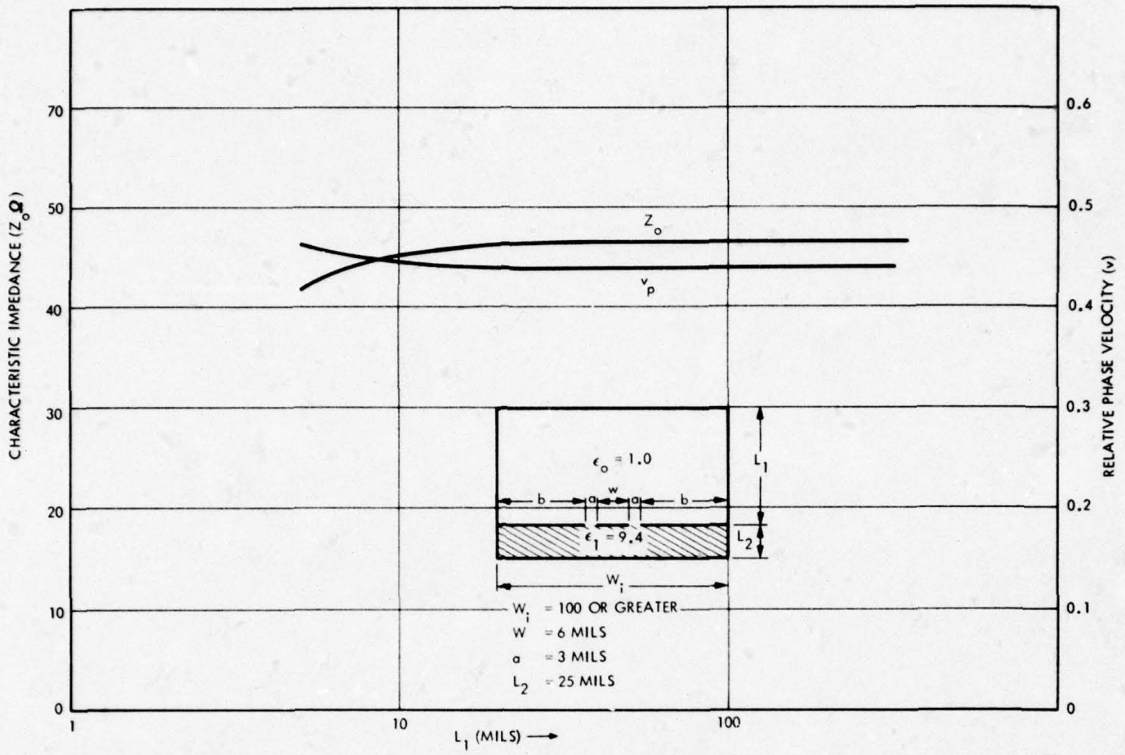


Figure 5-4. Variation of Characteristic Line Impedance and Relative Phase Velocity of a Coplanar Waveguide as a Function of Top Ground Plane Spacing Only

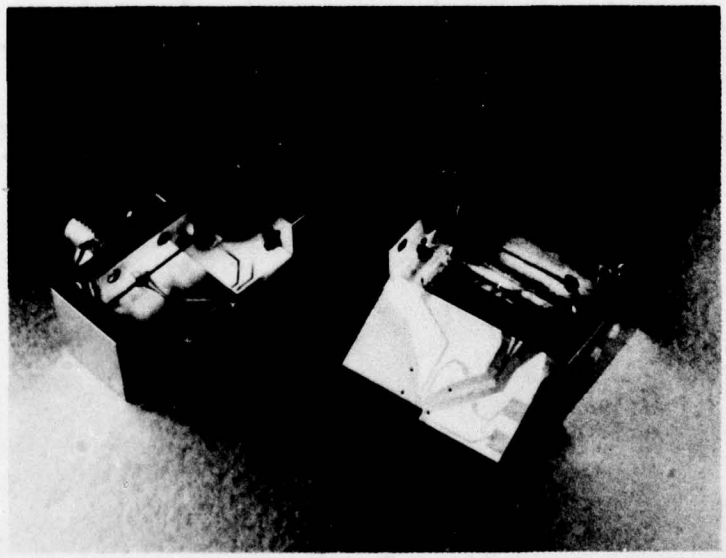


Figure 5-5. Demodulator Test Fixture and Substrate Assembly

5.1.2 Test Fixture Assembly

The substrates used in these circuits are made of alumina with the following metallization:

200 Å – NiCr
40 μin. – Au – vapor deposition
15 μin. – Au – strike (plate)
300 μin. – Cu – plate
54 μin. – Ni – plate
150 μin. – Au – plate

The copper plating allows the connectors to be soldered to the substrate. The Ni is a barrier to help prevent the surface Au and the Cu from alloying. Initially the alloying caused wire bonding problems, and the Au surface was added to help provide the proper bonding surface.

When the metallization is complete, the perimeters of the circuits are cut by a diamond saw on a horizontal cutting surface (Figure 5-6). The circuits are then cleaned and protected by plating tape.

The L-shaped portion has to be notched out of each half of the two substrates to form the rectangular hole for the IC chip. This is accomplished by placing the cutting surface perpendicular to the diamond blade and making several shallow cuts to the proper depth of the notch. After cutting, the circuits are degreased and cleaned in a J-100 solution to remove the cutting oil and tape gum from the surface. Each half of the circuit is then soldered into its respective fixture half. The external circuit connectors are soldered to their respective connector pads on the surface of the

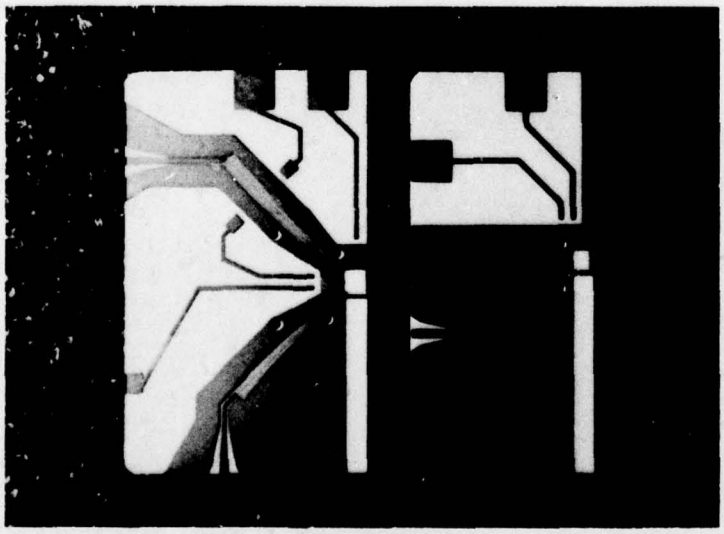


Figure 5-6. Demodulator Substrate Prior to Cutting the Notch for the IC Chip

substrate. The fixture and the substrate are cleaned again to remove excess flux and oil in preparing the surface for bonding.

The IC chip is aligned to the 2 mil RF lines on the substrate, adjusted to its proper height through the use of shims, and expoxied into place on the appropriate fixture half. The epoxy is dried at 150°C for 1-1/2 hours. The second half of the fixture is aligned to the 2 mil RF lines on the chip and the two fixture halves are bolted into place. Adjustments in the size of the hole required for the chip are made by sliding the two fixture halves to adjust one dimension and by adding shims between the fixture halves to adjust the other dimension.

Circuit connections are made by ultrasonic bonding 1 mil aluminum wire as shown in Figure 5-7.

5.1.3 Demodulator Data Detector Circuit

A data logic circuit was designed and constructed to help test the BPSK demodulator. This circuit completes the data demodulation by envelope detecting the AND gate outputs of the demodulator circuit. It consists of three basic building blocks, two detector diodes, a differential FET amplifier, and an RC lowpass filter. A schematic is shown in Figure 5-8.

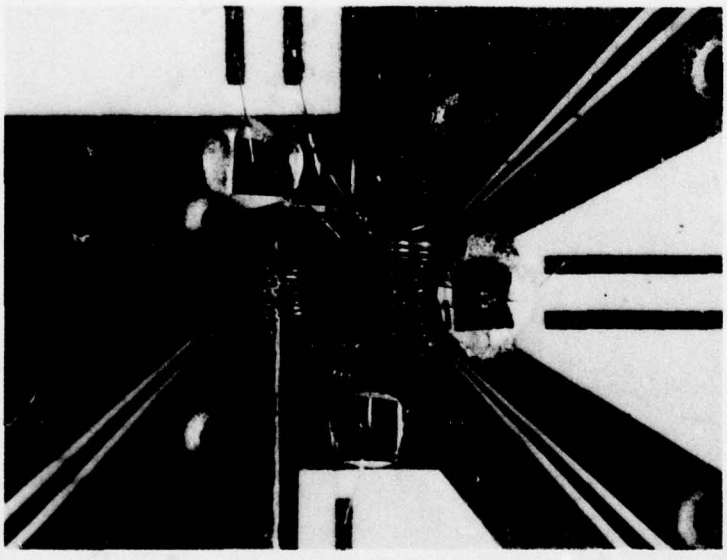


Figure 5-7. Example of Bonded Demodulator

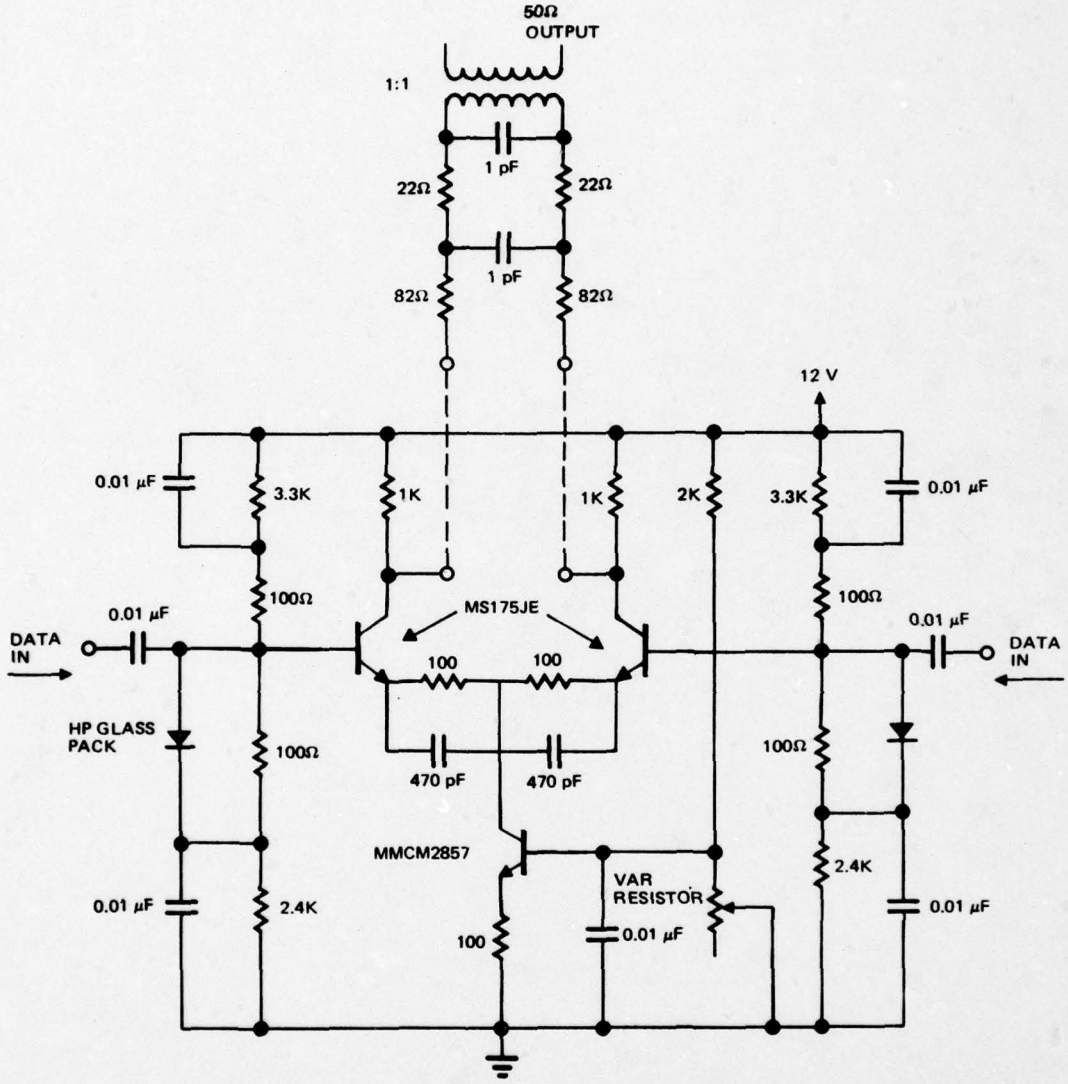


Figure 5-8. Schematic of Demod Data Detector Circuit

5.2 DESIGN VS FABRICATION COMPARISON

This section compares the fabricated modulator and demodulator IC chips to their respective design schematic values.

5.2.1 BPSK Modulator

The schematic for the modulator IC is presented in Figure 5-9. The resistor values for the circuit are shown with their calculated tolerances. Table 5-1 compares these design values with the typical measured values from wafers which yielded functioning modulators. Comparing Table 5-1 to Figure 5-9 shows that all of the individual resistors are within their design tolerance. Table 5-2 compares the design and actual bias conditions of the modulator circuits. The discrepancy between these bias conditions arises from the experimentally determined requirement for a higher ND product than originally planned. Table 5-3 shows the material design criteria discussed in Section 2 and the measured material parameters of the mod-23 wafer, the one which produced the best modulators.

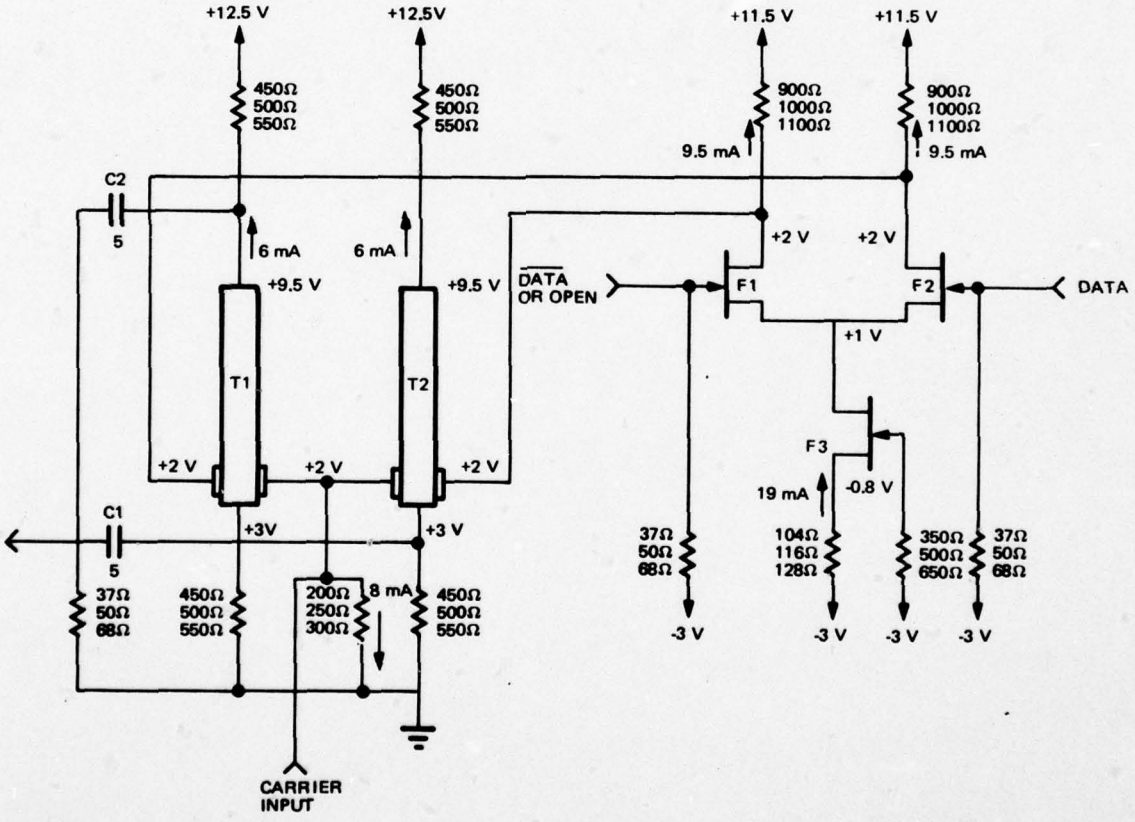


Figure 5-9. BPSK Modulator Schematic with Resistor Tolerances

Table 5-1. Modulator Resistor Value Comparison

Design (ohms)	Average (ohms)
50	45
116	100
500	469
1000	923

Table 5-2. Modulator Bias Comparison

	Design	Average
Anode voltage	+12.5 V	+14.70 V
Gate voltage	--	+ 3.41 V
Drain voltage	+11.5 V	+14.34 V
Source voltage	-3.00 V	-5.16 V
Anode current	6 mA	12 mA
Drain current (per device)	9.5 mA	12.5 mA
Source current	-19 mA	-25 mA

Table 5-3. Modulator Material Comparison

	Design	Actual (Mod-23)
Material	GaAs	GaAs
Channel concentration (atoms/cm^3)	$\geq 7 \times 10^{15}$	4×10^{16}
Channel thickness (μm)	≤ 1.5	0.6
Mobility	6200	≈ 5000

Using the minimum material design criteria shown here, the IDSS for FET's 1 and 2 in the circuit may be calculated to be 18.6 mA. Making the same calculation while using the measured material parameters, and allowing for some tolerances in the measured values, the IDSS for the FET's calculates to be 29.5 to 35.0 mA. The measured IDSS value for the mod-23 circuits was 33 mA. Therefore, with the higher IDSS values for the FET's one would expect the operating currents of the circuit to be higher also.

5.2.2 BPSK Demodulator

The schematic diagram for the demodulator IC is given in Figure 5-10. Tables 5-4 and 5-5 compare the design resistor values to the measured test values and the design bias conditions to the actual operating conditions. As Table 5-6 shows, the material specifications for the demodulator circuits are similar to those of the mod-23. This again explains the discrepancy in operating currents of the devices in demod-11. As discussed in Section 2, the actual value of the bulk resistors used in providing gate bias is unimportant, so long as it is large. The bulk resistors were designed to be 10K based on a ND product = 10^{12}, but the necessity to increase ND lowered the value of these resistors to about 5K, an effect which has no significance to the circuit operation.

Table 5-4. Demodulator Resistor Value Comparison

Design	Average
333 ohms	331 ohms
Bulk resistors	5000 ohms

Table 5-5. Typical Demodulator Bias Conditions

	Design	Average
Anode voltage	+10.5 V	+13.24 V
Gate 1 voltage	+ 1.0 V	+ 3.56 V
Gate 2 voltage	+ 1.0 V	+ 1.11 V
Anode current	6 mA	19.2 mA
Gate 1 current	5-6 mA	12.0 mA

Table 5-6. Demodulator Material Comparison

	Design	Actual (Demod-11)
Material	GaAs	GaAs
Channel concentration (atom/cm^3)	$\geq 7 \times 10^{15}$	3×10^{16}
Channel thickness (μm)	≤ 1.5	0.58
Mobility	6200	≈ 5000

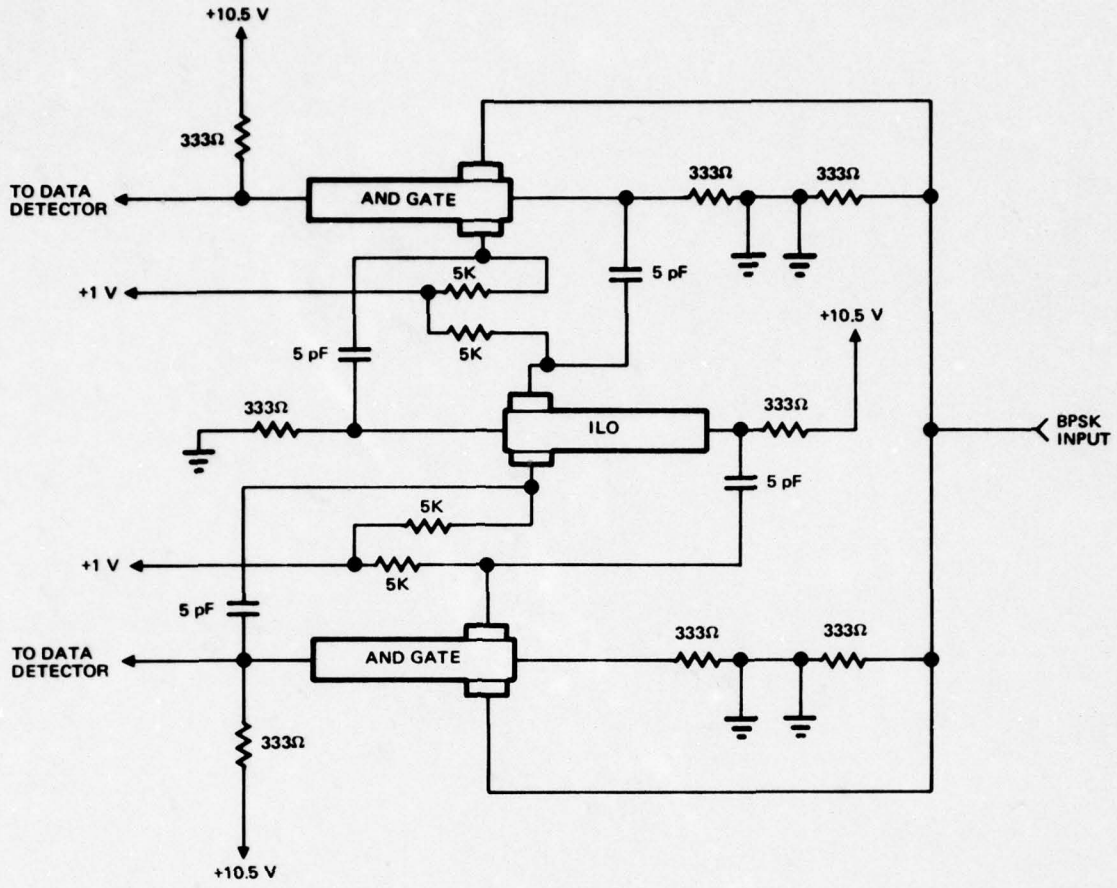


Figure 5-10. TED BPSK Demodulator Design

5.3 TEST SETUP AND PROCEDURES

5.3.1 Modulator

Figure 5-11 shows the test setup for the BPSK modulator and demonstrates the appropriate external bias points:

V_A = anode to cathode bias for both TED's

V_D = drain bias for the FET's in the differential pair

V_G = bias for the carrier input gates

V_{FG} = applies bias to the source and gate of the FET current source and to the gates of the differential pair FET's.

Figure 5-12 defines these points on the circuit schematic.

The modulator test procedures are as follows:

- Verify bonding and active chip components
- Establish approximate bias condition for the active devices via curve tracer measurements

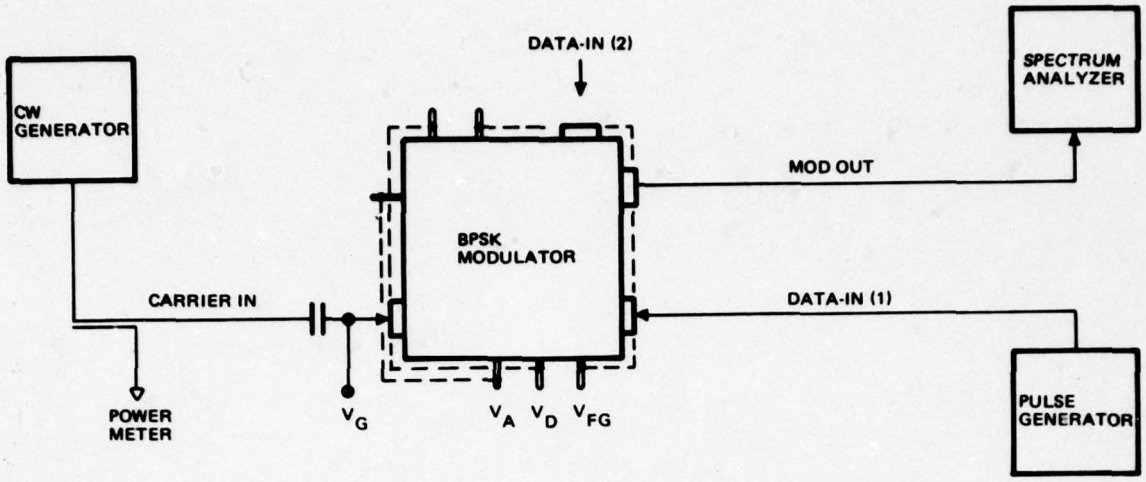


Figure 5-11. BPSK Modulator Test Setup

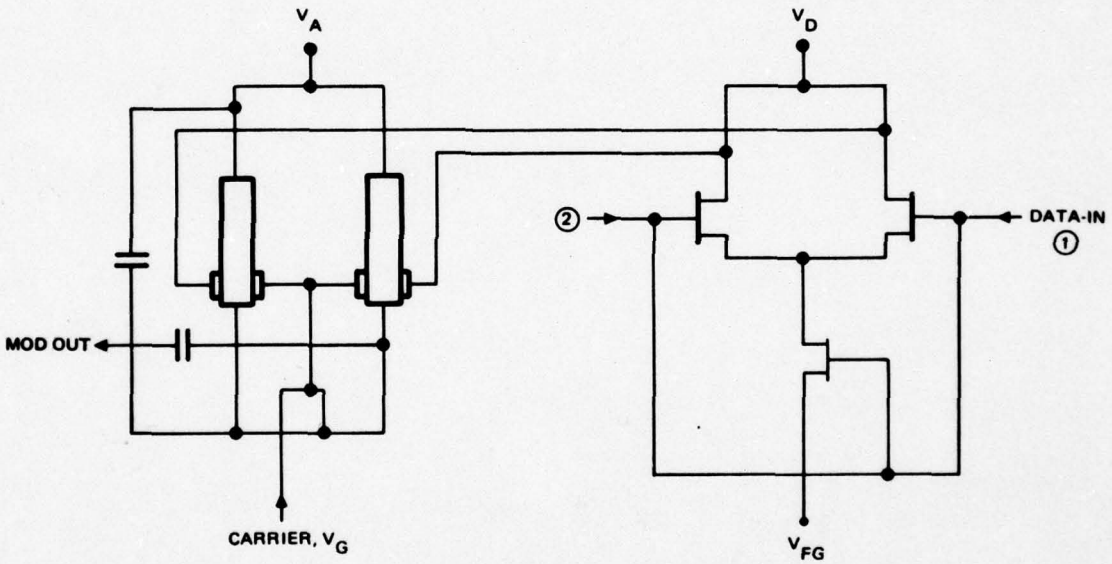


Figure 5-12. Modulator Schematic Showing Test Bias Points

- Externally connect appropriate dc bias points together
- Calibrate insertion loss of test setup
- Using the test setup shown in Figure 5-11 and biasing the anodes of the TED's first, adjust gate potentials of both the TED's and the FET's to provide the appropriate trigger sensitivity for the carrier and data inputs
- Verify operation and harmonic content of modulator over a range of data rates by examining the spectrum analyzer display.

5.3.2 Demodulator

Figures 5-13 and 5-14 show the demodulator test configuration and the test bias points. Figure 5-15 shows the test setup for the combined mod/demod test.

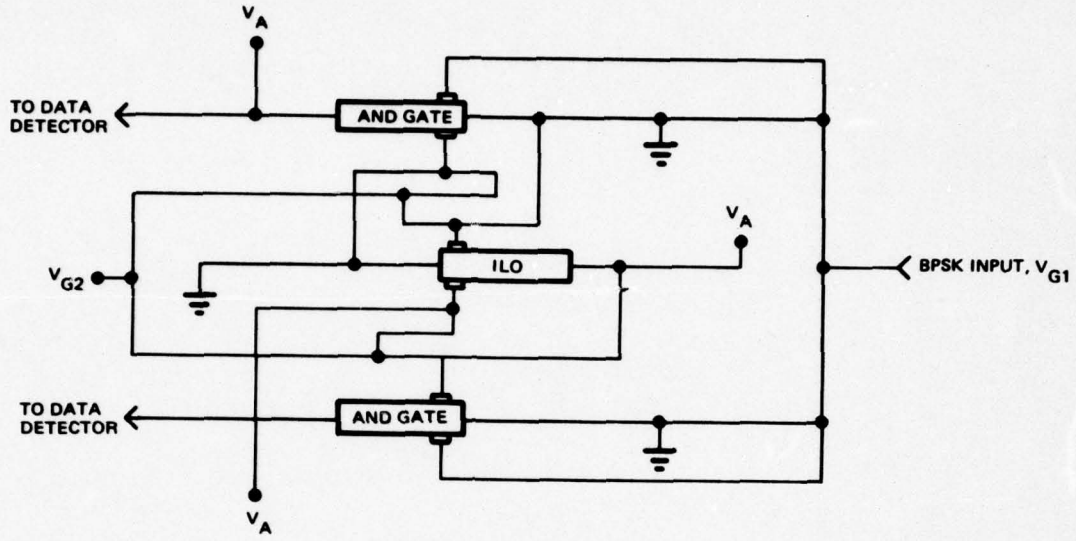


Figure 5-13. Demodulator Schematic Showing Test Bias Points

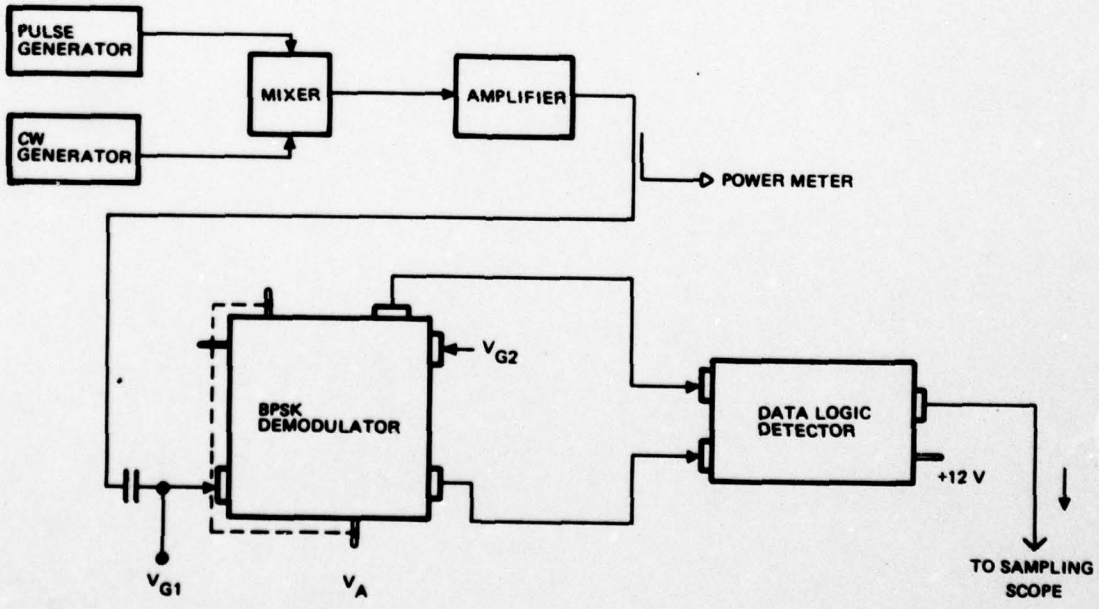


Figure 5-14. BPSK Demodulator Test Setup

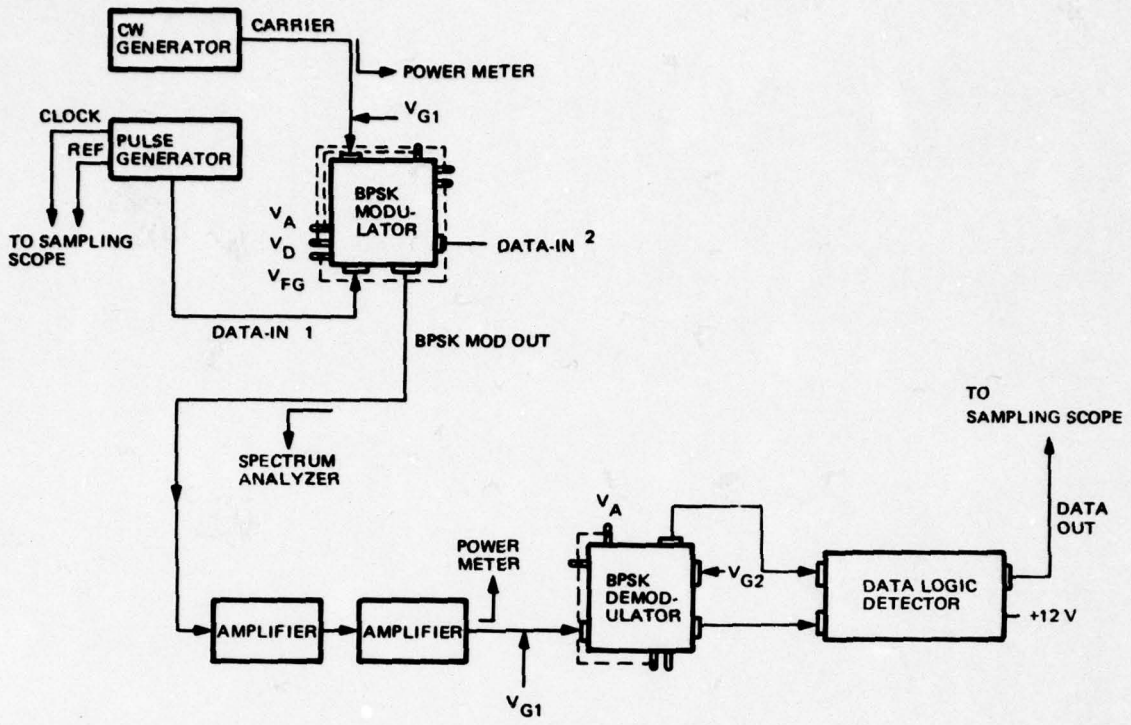


Figure 5-15. Mod/Demod Test Configuration

The demodulator test procedures are as follows:

- Verify bond connections and active chip components
- Establish approximate bias conditions for the TED's via the curve tracer
- Develop a modulated input signal as shown in test setup of Figure 5-14
- Adjust gate biases to give maximum trigger sensitivity
- Envelope detect the AND gate outputs with the data logic circuit shown in Figure 5-8
- Compare demodulated signal to data input using sampling scope
- Verify operation over a range of data rates and carrier frequencies.

5.4 TEST RESULTS

5.4.1 Modulator

After the IC chips were mounted and bonded into their respective fixtures, the impedance mismatch between the chip and each 50 ohm transmission line was investigated using a time domain reflectometer. The measurements were made with a Hewlett-Packard 1815A sampling plug-in and a 1817A sampling head, which provided a 50 ohm terminated test system and sampling capabilities to 12.4 GHz. The purpose of this measurement was twofold: it provided VSWR information used in the analysis of the circuit and it gave an indication of the quality of the 50 ohm transmission line and the bond at the chip.

Figure 5-16 is a representative photograph of the measured data from the time domain reflectometer. Table 5-7 tabulates this information in the form of VSWR for each RF port in the circuit.

Table 5-7. Typical Impedance Mismatch in Modulator Circuits

Circuit	VSWR (:1)
Carrier input port	3.5
Modulation output port	1.5
Data input port	1.2
Data input port	1.3

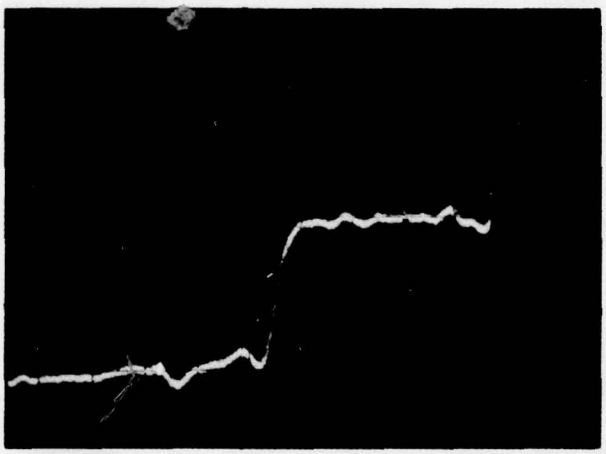
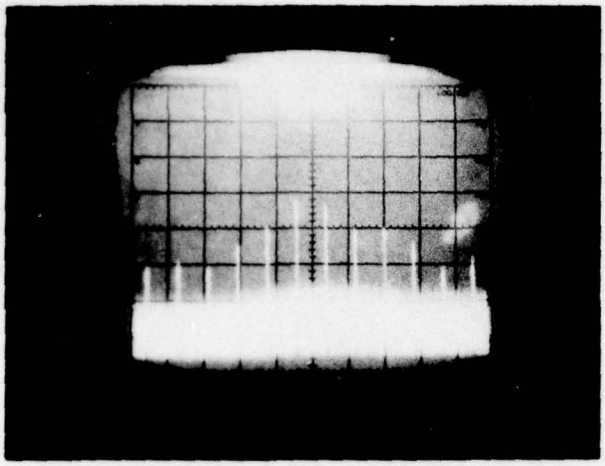


Figure 5-16. Time Domain Reflector Measurements Mod-L23 RF Input Port

Although these circuits were capable of modulating at data rates from 0-1.4 Gbps, proper carrier suppression was difficult to obtain. This may be due in part to limitations of the pulse generators used to supply the data signal to the modulators. While several manufacturers supply square wave generators capable of operation to at least 500 MHz, none of this has a risk time of less than 250 psec, and all exhibit considerable distortion when operated above half their maximum frequency. A discussion of the contribution of poor square wave rise times to poor carrier suppression as given in Section 5.5.

At low data rates the output waveform from the pulse generator was reasonably square. Figure 5-17 shows an example of the modulator output at a data rate of 16 Mbps. Note that the spectral output is as expected with good carrier suppression and only odd harmonics are present in the spectrum.

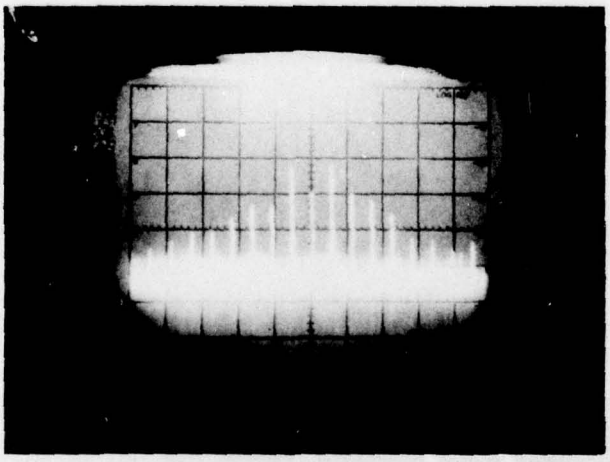


Data rate: 16 Mbps
Frequency out: 7.9 GHz
Frequency in: 15.8 GHz
Power in: 4 dBm
Carrier suppression: ≥22 dBm

Scale: 20 MHz/div

Figure 5-17. Mod-L23-3 – Low Data Rate Input with Good Carrier Suppression and Only Odd Harmonics

As the data rate was increased, the output spectrum of the modulator changed to a spectrum similar to the one shown in Figure 5-18. The presence of the carrier and the even harmonics in the spectral output of the modulator was often observed at the higher data rate modulations. Both Figures 5-18 and 5-19 demonstrate low level operation of the modulator. The -15 dBm RF input level shown in Figure 5-19 was the minimum power input obtained for the modulator circuit. (An example of high data rate modulation is shown in Figure 5-24.) A summary of results from the modulator tests is given in Table 5-8.



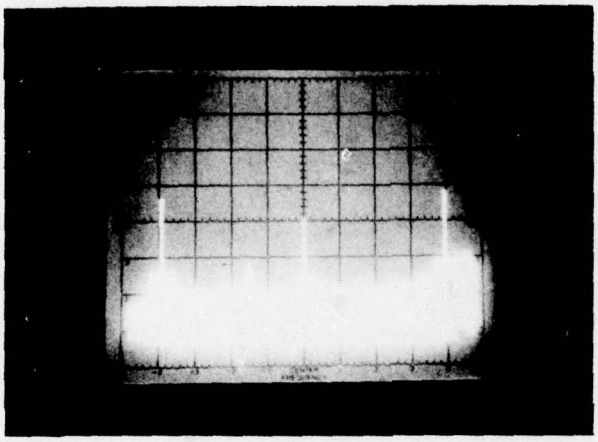
Data rate: 60 Mbps
Frequency out: 7.85 GHz
Frequency in: 15.7 GHz
Power in: -11 dBm

Scale: 50 MHz/div

Figure 5-18. Mod-L23-3 – Low Level Input, with the Presence of the Carrier Signal and the Even Harmonics

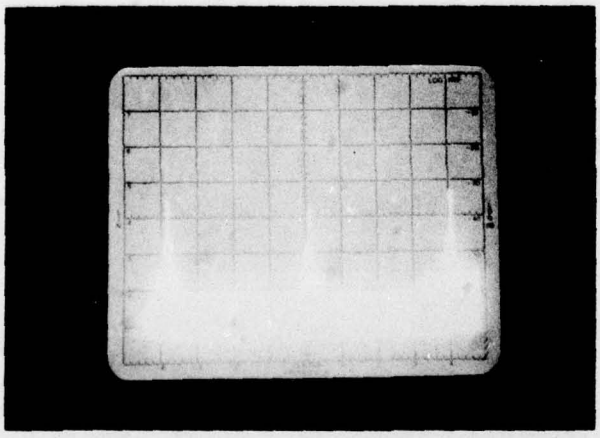
Table 5-8. Summary of BPSK Modulator Test Results

Minimum P_{in} to trigger	-15 dBm
Data rate	0 to 1.4 Gbps
Average dc power	650 mW (420 mW minimum)
Frequency of oscillation	4.5 to 8.5 GHz
Isolation:	
Carrier input to mod output port	24 dB
Carrier input to data input port	36 dB



Power in: -1 dBm

Scale: 50 MHz/div



Power in: -15 dBm

Frequency: 7.85 GHz
Data rate: 400 Mbps

*Scope in storage mode.

Figure 5-19. Mod-L23-3 — Low Level Input and Medium Data Rate

5.4.2 Demodulator

The demodulator test circuits were subject to the same time domain reflectometer measurements as the modulator circuits. A representative photograph of this measured data is shown in Figure 5-20. Table 5-9 tabulates this information in VSWR for each RF port in the circuit.

Table 5-9. Typical Impedance Mismatch in Demodulator Circuits

Circuit	VSWR (:1)
Modulation input port	3.5
AND gate output port 1	4.0
AND gate output port 2	4.0

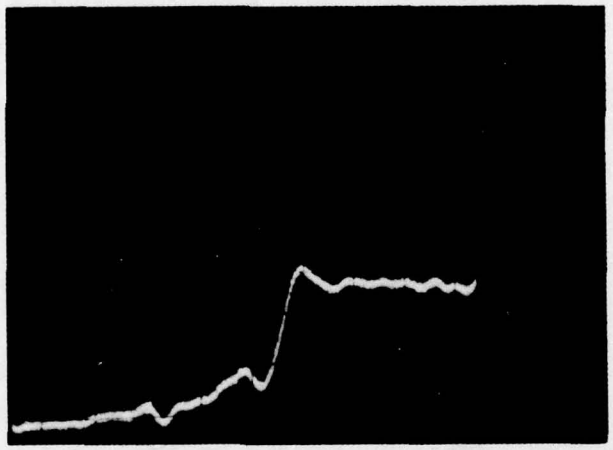
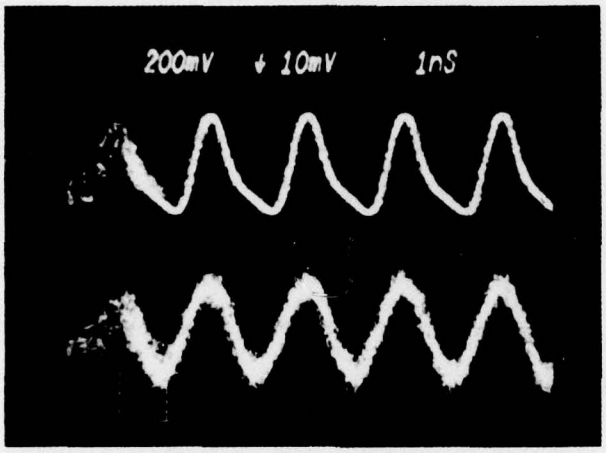


Figure 5-20. Example of TDR Measurements of Demod Circuit

Figures 5-21, 5-22, and 5-23 show representative outputs from the demodulator that demonstrate its 1 Gbps demodulation capability and its ability to operate at relatively low input power. An input power of -13 dBm was the lowest operational input level obtained (Figure 5-23). A summary of results from the demodulator tests is given in Table 5-10.

Table 5-10. Summary of BPSK Demodulator Results

Minimum P_{in} to triggers	-13 dBm
Data rate	0-1.6 Gbps
Average dc power	275 mW (208 mW min)
Frequency of operation	4 to 11 Ghz
Isolation – BPSK input to data output	26 dB

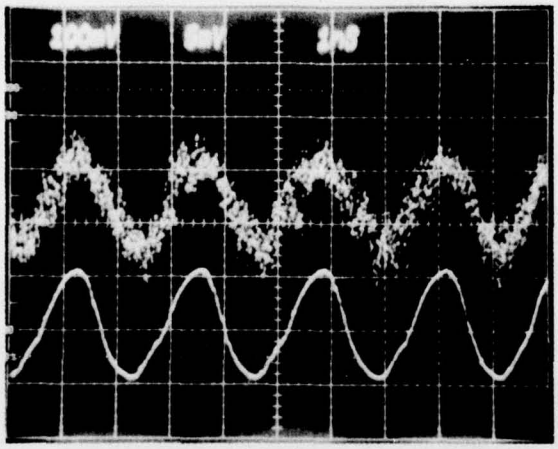


Data in

Data out

Data Rate: 1 Gbps
Modulation frequency: 4-11 Gbps
Power in: +7 dBm

Figure 5-21. Demod-L11-3

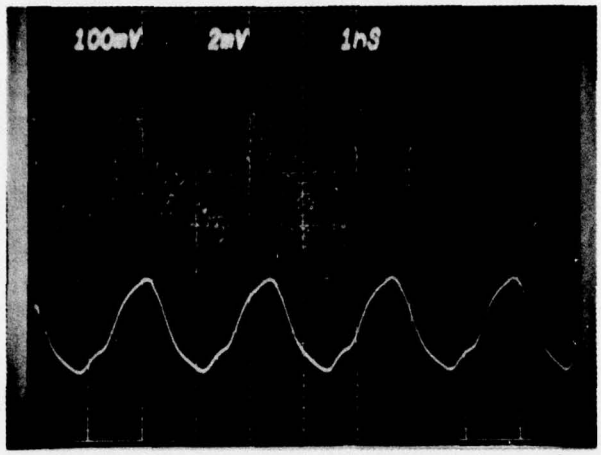


Data out

Data in

Data rate: 840 Mbps
Modulation frequency: 4-8 GHz
Power in: 0 dBm

Figure 22. Demod-L11-3



Data out

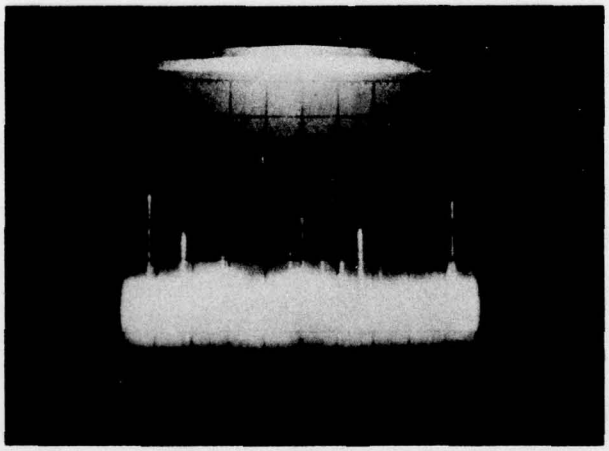
Data in

Data rate: 840 Mbps
Modulation frequency: 4-8 GHz
Power in: -13 dBm

Figure 5-23. Demod-L11-2 — Low Level Input

5.4.3 Modulator/Demodulator

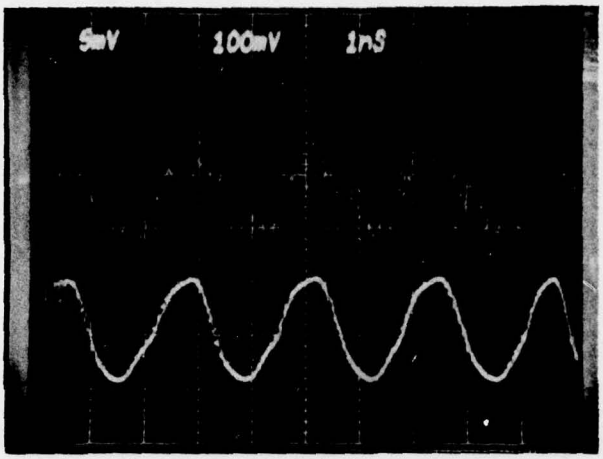
Using the test setup shown in Figure 5-14, the mixer used previously to produce the modulation input in the demodulator testing was replaced by the modulator circuit. Figure 5-24 shows the modulator output before it was amplified. The modulation rate in this instance was 840 Mbps. Figure 5-25 compares the demodulator output to the modulator data input for different power levels into the demodulator.



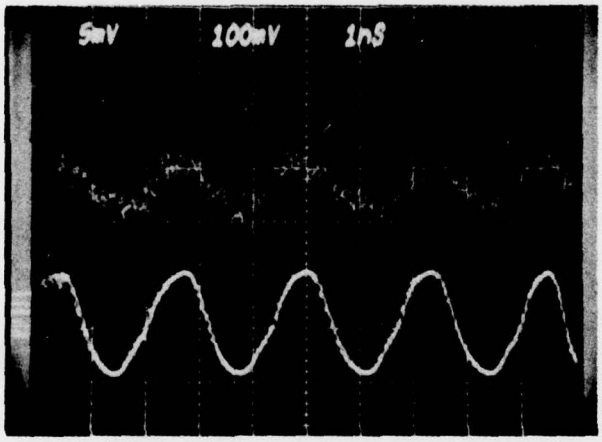
Scale: 100 MHz/div

Data rate: 840 Mbps
Frequency out: 7.85 GHz
Frequency in: 15.7 GHz
Power into mod: -3 dBm

Figure 5-24. Modulator Output of Mod-Demod Combination



a) Power into Demod: +5 dBm



b) Power into Demod: 0 dBm

Figure 5-25. Demodulator Output of Mod/Demod Combination

In the design of the modulator and demodulator circuits, some temporary tradeoffs had to be made between minimizing dc power and minimizing the mismatch at some of the input and output ports. For example, as discussed in Section 2, the design of the modulator circuit requires a dc voltage on the RF input gates of about 2 volts. Since the gate circuit of the RF input port draws very little current, the resistor to ground used to establish the 2 volts on the gates becomes an important factor in determining both the dc power and the mismatch at the input port. Lowering this resistance to match the input would increase the power consumption of the circuit, whereas raising this resistance to reduce power consumption would increase the mismatch at the input. In situations where this circumstance arose in the design of these circuits, a resistance value was chosen to provide a reasonable compromise between the desired parameters. It will be possible in the future to further RF match these ports either on the chip itself or on the external test circuitry around the chip.

Due to the mismatches that are present at the input ports of the modulator and the demodulator, a higher RF input power level is required to achieve the desired operation from the circuits. However, since the mismatch can be measured, it is possible to determine if the devices in the circuit are operating at optimum conditions.

To determine a theoretical value of the amount of power required to operate these circuits, several test TED's were diced from a mod-21 wafer and mounted in 50-ohm single device test fixtures. These TED's were then tested to determine the minimum trigger sensitivity of the device. This was determined to be about -30 dBm. The impedance of the gate was measured using a network analyzer. Knowing this impedance and the minimum power required to trigger the gate, the voltage required to trigger the gate can be calculated as follows

$$\text{Power} = V^2/2R \tag{5.1}$$

therefore

$$V = (P2R)^{1/2} = 0.1\ V \tag{5.2}$$

where

$P = -30$ dBm $= 1 \times 10^{-6}$ watts

$R = 5000$ ohms (measure real part of gate impedance)

Due to the similarity in the design of these test TED's and the TED's in the modulator circuit, one may assume that the TED's in the modulator circuit will also have a minimum voltage sensitivity of about 0.1 volt. Therefore, the power required to present this voltage to the gate of the modulator TED's may be calculated in a similar manner. Figure 5-26 shows the simplified equivalent circuit looking into the carrier input port. Therefore

$$P_T = \frac{V^2}{2R} = \frac{0.01}{600} = 1.67 \times 10^{-5}\ \text{watts} = 0.0167\ \text{mW} \tag{5.3}$$

where P_T = the power to the TED's.

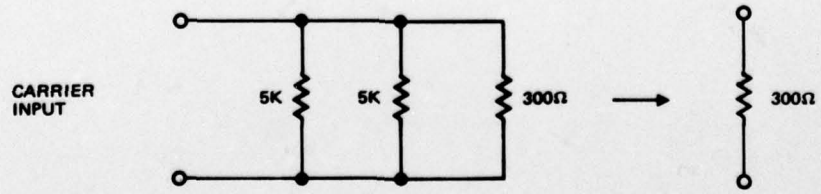


Figure 5-26. Carrier Input Equivalent Circuit for the BPSK Modulator

From the TDR measurements discussed earlier, the reflection coefficient of the carrier input port was found to be about 0.56 for all of the modulator circuits (Table 5-7). Since

$$\rho = \sqrt{\frac{P_{reflected}}{P_{incident}}} \tag{5.4}$$

the incident power required at the input port to produce a 0.1 volt change at the gate can be calculated

$$P_R = 0.314\ (P_{inc}) \tag{5.5}$$

$$P_T = P_{inc} - P_R \tag{5.6}$$

$$P_{inc} = P_T/0.686 = 0.024\ mW$$

$$P_{inc} = -16.2\ dBm \tag{5.7}$$

Therefore, for the modulator circuit, the minimum theoretical power input to the carrier port for the device to trigger is -16 dBm. This compares to the -15 dBm minimum power input measured in the lab (Table 5-8).

Using the same procedure, a calculation can be made for the demodulator circuit. Figure 5-27 represents the equivalent for the demodulator looking into the RF input. Therefore

$$P_T = \frac{V^2}{2R} = \frac{0.01}{2\ (156)} \tag{5.8}$$

$$P_T = 0.0321\ dBm$$

$$P_R = 0.314\ P_{inc} \tag{5.9}$$

$$P_T = P_{inc} - P_R \tag{5.10}$$

and

$$P_{inc} = P_T/0.686 = -13.3\ dBm \tag{5.11}$$

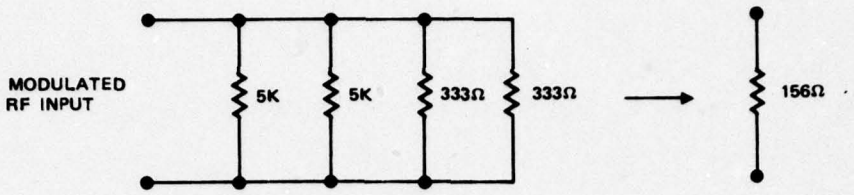


Figure 5-27. Input Equivalent Circuit for the BPSK Demodulator

Again, this theoretical value for the minimum input power compares well with the minimum operational input power measured for the demodulator circuit (Table 5-10). The results from this investigation indicate that both the modulator and demodulator circuit TED's were capable of operating close to their maximum sensitivity levels.

5.5 ANALYSIS OF RESULTS

The BPSK modulated output from this circuit is produced by voltage controlling the outputs of two 180° out-of-phase signal generators, the TED's. Although the data input to a BPSK modulator is usually not a periodic waveform, such a waveform may be used to model and test its operation. The output signal from the modulator can be modeled by a multiplication operation between the carrier signal and the data signal. The carrier frequency represents the frequency of oscillation of the TED's. Since the TED's have only two states, on or off, the data information signal used to trigger the TED's can be represented by a waveform that represents the state of the TED's as a function of time. This is an acceptable representation of the data signal since the TED's are set up to be on for one data state and off for the other data state. The data signal for each device can be represented as shown in Figure 5-28, where K_1 and K_2 are the respective amplitudes of the TED outputs and T is the period of the data signal. Note that the 180° phase shift between the two outputs is represented by the minus amplitude of y(t). Each of the waveforms shown in Figure 5-28 can be expressed mathematically by a Fourier series as shown in equations (5.12) and (5.13).

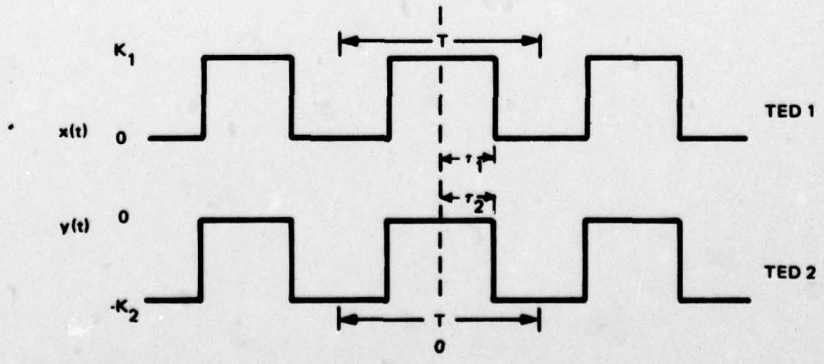


Figure 5-28. Data Signals

$$x(t) = A_0 + \sum_{n=1}^{\infty} A_n \cos n\omega_1 t + C_n \sin n\omega_1 t \tag{5.12}$$

$$y(t) = B_0 + \sum_{n=1}^{\infty} B_n \cos n\omega_1(t) + D_n \sin n\omega_1 t \tag{5.13}$$

where

$$A_0 = \frac{1}{T} \int_{-T/2}^{T/2} x(t)\, dt = \frac{2 K_1 Z_1}{T} \tag{5.14}$$

$$A_n = \frac{2}{T} \int_{-T/2}^{T/2} K_1 \cos n\omega_1 t\, dt = \frac{2 K_1}{n\pi} \left[\sin n\omega_1 \tau_1\right] \tag{5.15}$$

$$C_n = \frac{2}{T} \int_{-T/2}^{T/2} K_1 \sin n\omega_1 t\, dt = 0 \tag{5.16}$$

$$B_0 = \frac{2}{T} \int_{-T/2}^{T/2} y(t)\, dt = -\frac{K_2}{T} \left[T - 2\tau_2\right] \tag{5.17}$$

$$B_n = \frac{2}{T} \int_{-T/2}^{T/2} -K_2 \cos n\omega_1 t\, dt = \frac{2 K_2}{n\pi_1} \left[\sin n\omega_1 \tau_2\right] \tag{5.18}$$

$$D_n = \frac{2}{T} \int_{-T/2}^{T/2} -K_2 \sin n\omega_1 t\, dt = 0 \tag{5.19}$$

Now, letting $z(t) = \cos \omega_c t$, the carrier signal, the output waveform from the modulator, P(t), may be expressed as

$$P(t) = z(t)\, x(t) + z(t)\, y(t) = z(t)\, [x(t) + y(t)] \tag{5.20}$$

Substituting

$$P(t) = \cos \omega_c t \left[\left(\frac{2 K_1 \tau_1}{T} + \frac{2 K_2 \tau_2}{T} - K_2\right) + \sum_{n=1}^{\infty} \frac{2}{n\pi} \left(K_1 \sin n\omega_1 \tau_1 + K_2 \sin n\omega_1 \tau_2\right) \cos n\omega_1 t\right] \tag{5.21}$$

Performing the multiplication

$$P(t) = \left(\frac{2K_1\,\tau_1 + K_2\,\tau_2}{T} - K_2\right)\cos\,\omega_c t + \sum_{n=1}^{\infty}\frac{2}{n\pi}\left[(K_1 \sin n\omega_1\,\tau_1 + K_2 \sin n\,\omega_1\tau_2)\left(\cos\,(\omega_c + n\,\omega_1)\,t + \cos\,(\omega_c - n\,\omega_1)\,t\right)\right] \tag{5.22}$$

Simplifying

$$P(t) = P_0 \cos\,\omega_{ct} + \sum_{n=1}^{\infty}\left[P_1\left(\cos(\omega_c + n\,\omega_1)t + \cos(\omega_c - n\,\omega_1)\,t\right)\right] \tag{5.23}$$

where

$$P_0 = \left(\frac{2\,K_1\,\tau_1}{T} + \frac{2\,K_2\,\tau_2}{T} - K_2\right) \tag{5.24}$$

$$P_1 = \frac{2}{n\pi}\left[K_1 \sin n\,\omega_1\,\tau_1 + K_2 \sin n\,\omega_1\,\tau_2\right] \tag{5.25}$$

Equation (5.23) describes the spectral output of the modulator circuit. Under ideal operating conditions, a BPSK modulator will have only the summation of the

$$P_1\left[\left(\cos\,(\omega_c + n\,\omega_1)\,t\right) + \left(\cos\,(\omega_c - n\omega_1)\,t\right)\right]$$

term in its output. No carrier signal would be present. However, equation (5.23) shows that it is possible to have a carrier frequency present in the output of the modulator under certain conditions. Note that when $\tau_1 = \tau_2 = T/4$ and $|K_1| = |K_2|$ the carrier component in the output goes to zero. This means that the outputs of the two TED's, T_1 and T_2 (Figure 5-9), must be equal in amplitude and only one TED can be on at a time. Any other mode of operation from this circuit will tend to produce a carrier component in the output spectrum.

Table 5-11 considers several possible modes of operation of the modulator circuit. Investigation into these different operating conditions using equation (5.23) indicates the presence of the carrier frequency in the output spectrum of all but the first case.

Table 5-11. Possible Operating Modes of Modulator Due to Variations in TED Operation

Perfect operation
$K_1 = K_2$ and $\tau_1 = \tau_2 = T/4$
One TED output larger
$K_1 \neq K_2$ and $\tau_1 = \tau_2 = T/4$
TED's on for overlapping times
$K_1 = K_2$ and $\tau_1 > T/4 > \tau_2$
$K_1 \neq K_2$ and $\tau_1 > T/4 > \tau_2$
TED's on for underlapping times
$K_1 = K_2$ and $\tau_1 < T/4 < \tau_2$
$K_1 \neq K_2$ and $\tau_1 < T/4 < \tau_2$

Considering the possible variations in concentration and channel thickness of two TED's on the same chip, it is reasonable to assume that K_1 is approximately equal to K_2. As for the conditions of having the TED's on for overlapping or underlapping times (Table 5-11), one must consider the possible operation of the two TED's and the shape of the data signal being used to trigger them. It is possible to have two TED's turn on at different gate potentials and off at different gate potentials. For example, assume the following two data signals trigger the two TED gates at the levels shown in Figures 5-29 and 5-30. Figure 5-30 indicates that for short periods of time it is possible to have both TED's on at the same time. The probability of having them on at the same time will depend on the rise time of the data signal being used to trigger the TED's and the biasing condition described above. If the rise time of the data signal is slower than the time it takes for a domain to traverse the channel of the device, it will be possible to launch another domain in the first TED and have it traverse the channel at the same time that the second TED's domain is being launched. Hence both devices are on at the same time. The time in which both TED's are on is represented by the difference between τ_1 and τ_2 in the previous analysis. As equations (5.23), (5.24), and (5.25) show, the value of τ_1 and τ_2 has a substantial effect on the magnitude of the carrier and harmonic frequencies in the spectral output of the modulator.

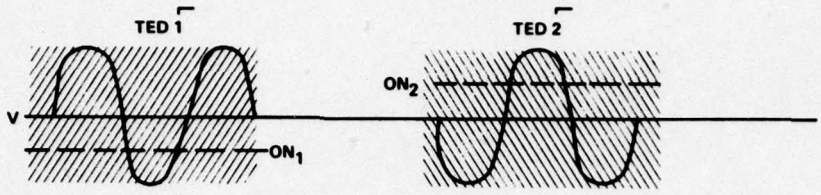


Figure 5-29. Possible Required Biases for Triggering Two TED's

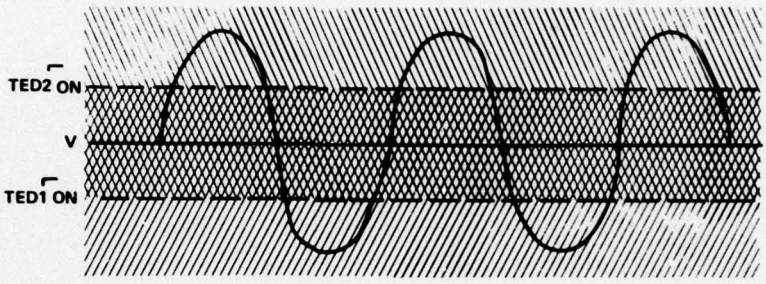


Figure 5-30. Possible Overlapping of TED 1 and TED 2

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